MT6589 HSPA+ Smartphone Application Processor Technical Brief

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1 System Overview

MT6589 is a highly integrated baseband platform incorporating both modem and application processing subsystems to enable 3G smart phone applications. The chip integrates a Quad-core ARM® Cortex-A7 MPCore™ operating up to 1.2GHz, an ARM® Cortex-R4 MCU and a powerful multi-standard video accelerator. The MT6589 interfaces to NAND flash memory, 32-bit LPDDR2 for optimal performance and also supports booting from SLC NAND or eMMC to minimize the overall BOM cost. In addition, an extensive set of interfaces and connectivity peripherals are included to interface to cameras, touch-screen displays, MMC/SD cards and external Bluetooth, WiLAN and GPS modules.

The application processor, a Quad-core ARM® Cortex-A7 MPCore™ which includes a NEON multimedia processing engine, offers processing power necessary to support the latest OpenOS along with its demanding applications such as web browsing, email, GPS navigation and games. All are viewed on a high resolution touch screen display with graphics enhanced by the 2D and 3D graphics acceleration. The multi-standard video accelerator and an advanced audio subsystem are also included to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders such as H.264 and MPEG-4. Audio supports include FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR vocoders, polyphonic ringtones and advanced audio functions such as echo cancellation, hands-free speakerphone operation and noise cancellation.

An ARM® Cortex-R4, DSP, and 2G and 3G coprocessors provide a powerful modem subsystem capable of supporting Category 24 (42.2 Mbps) HSDPA downlink and Category 7 (11.5 Mbps) HSUPA uplink data rates, as well as Class 12 GPRS and EDGE.

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1.1 Platform Features

- **General**
  - Smartphone two MCU subsystems architecture
  - SLC NAND flash and eMMC bootloader

- **AP MCU subsystem**
  - Quad-core ARM® Cortex-A7 MPCore™ operating at 1.2GHz
  - NEON multimedia processing engine with SIMDv2/VFPv4 ISA support
  - 32KB L1 I-cache and 32KB L1 D-cache
  - 1MB unified L2 cache
  - DVFS technology with adaptive operating voltage from 0.95V to 1.26V

- **MD MCU subsystem**
  - ARM® Cortex-R4 processor with maximum 480MHz operation frequency
  - 64KB I-cache, 32KB D-cache
  - 256KB TCM (tightly-coupled memory)
  - DSP for running modem/voice tasks, with maximum 240MHz operation frequency
  - High-performance AXI and AHB bus
  - General DMA engine and dedicated DMA channels for peripheral data transfer
  - Watchdog timer for system error recovery
  - Power management for clock gating control

- **MD external interfaces**
  - Supports dual SIM/USIM interface
  - Interface pins with RF and radio-related peripherals (antenna tuner, PA, …)
  - UART for modem logging/debugging purpose

- **External memory interface**
  - Supports LPDDR2 up to 2GB
  - 32-bit data bus width
  - Memory clock up to 533MHz
  - Supports self-refresh/partial self-refresh mode
  - Low-power operation
  - Programmable slew rate for memory controller's IO pads
  - Supports dual rank memory device
  - Advanced bandwidth arbitration control

- **Security**
  - ARM® TrustZone® Security

- **Connectivity**
  - USB2.0 high-speed OTG supporting 15 Tx and 15 Rx endpoints
  - USB2.0 full-speed host
  - NAND flash controller supporting NAND bootable, iNAND2® and MoviNAND®
  - 4 UART for GPS, BT, FM-RDS, modem and debugging interfaces
  - IrDA FIR/MIR/SIR
  - SPI for external device
  - 7 I2C to control peripheral devices, e.g. CMOS image sensor, LCM or FM receiver module
  - I2S for connection with optional external hi-end audio codec
  - GPIOs
  - 4 sets of memory card controllers supporting SD/SDHC/MS/MSPRO/MMC and SDIO2.0/3.0 protocols

- **Operating conditions**
  - Core voltage: 1.05V
  - Processor DVFS voltage: 0.95V ~ 1.26V (Typ. 1.05V; sleep mode 0.85V)
  - Processor SRAM voltage: 1.05V ~ 1.26V (Typ. 1.05V; sleep mode 0.85V)

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- GPU voltage: 1.05V
- I/O voltage: 1.8V/2.8V/3.3V
- Memory: 1.2V/1.8V/1.35V/1.5V/1.25V
- NAND: 1.8V/2.8V
- LCM interface: 1.8V
- Clock source: 26MHz, 32.768kHz

- **Package**
  - Type: FCCSP
  - 11.8mm x 11.8mm
  - Height: 1.0mm maximum
  - Ball count: 515 ballsc
  - Ball pitch: 0.4mm

1.2 MODEM Features

- **3G UMTS FDD supported features (with MT6167)**
  - 3G modem supports most main features in 3GPP Release 7 and Release 8
  - CPC (DTX in CELL_DCH, UL DRX DL DRX), HS-SCCH-less, HS-DSCH
  - Dual cell operation
  - MAC-ehs
  - Two DRX (receiver diversity) schemes in URA_PCH and CELL_PCH
  - Uplink Cat. 7 (16QAM), throughput up to 11.5Mbps
  - Downlink Cat. 24 (64QAM, dual-cell HSDPA), throughput up to 42.2Mbps
  - Fast dormancy
  - ETWS
  - Network selection enhancements

- **3G TDD supported features (with MT6168)**
  - TD-SCDMA/HSDPA/HSUPA baseband
  - Supports TD-SCDMA Bands 34, 39 & 40 and Quad band GSM/EDGE
  - Circuit-switched voice and data, and packet-switched data
  - 384/384Kbps class in UL/DL for TD-SCDMA
  - TD-HSDPA: 2.8Mbps DL (Cat.14)
  - TD-HSUPA: 2.2Mbps UL (Cat.6)
  - F8/F9 ciphering/integrity protection

- **Radio interface and baseband front-end**
  - High dynamic range delta-sigma ADC converts the downlink analog I and Q signals to digital baseband
  - 10-bit D/A converter for Automatic Power Control (APC)
  - Programmable radio Rx filter with adaptive gain control
  - Dedicated Rx filter for FB acquisition
  - Baseband Parallel Interface (BPI) with programmable driving strength (shared by 2G & 3G modem)
  - Supports multi-band

- **GSM modem and voice CODEC**
  - Dial tone generation
  - Noise reduction
  - Echo suppression
  - Advanced sidetone oscillation reduction
  - Digital sidetone generator with programmable gain
  - Two programmable acoustic compensation filters
  - GSM quad vocoders for adaptive multirate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
  - GSM channel coding, equalization and A5/1, A5/2 and A5/3 ciphering
  - GPRS GEA1, GEA2 and GEA3 ciphering
  - Programmable GSM/GPRS/EDGE modem
  - Packet switched data with CS1/CS2/CS3/CS4 coding schemes

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- GSM circuit switch data
- GPRS/EDGE Class 12
- Supports SAIC (single antenna interference cancellation) technology
- Supports VAMOS (Voice services over Adaptive Multi-user channels on One Slot) technology in R9 spec

1.3 Multimedia Features

- **Display**
  - Supports landscape or portrait panel resolution up to WXGA (1280x800)
  - Supports 8/9/16/18/24-bit host interface (MIPI DBI)
  - Supports 8/9/16/24/32-bit serial interfaces
  - Supports 16/18/24-bit RGB interfaces (MIPI DPI)
  - MIPI DSI interface (4 data lanes)
  - Embedded LCD gamma correction
  - Supports true colors
  - 4 overlay layers with per-pixel alpha channel and gamma table
  - Supports spatial and temporal dithering
  - Supports side-by-side format output to stereo 3D panel in both portrait and landscape modes
  - Supports external HDMI/MHL Tx bridge with 720p video output
  - Supports color enhancement
  - Supports adaptive contrast enhancement
  - Supports image/video/graphic sharpness enhancement
  - Supports dynamic backlight scaling

- **Graphics**
  - OpenGL ES 1.1/2.0 3D graphic accelerator capable of processing 50M tri/sec and 572M pixel/sec @ 286MHz (effective pixel rate: 1,430M pixel/sec.)
  - OpenVG1.1 vector graphics accelerator
  - 2D graphics hardware accelerator

- **Image**
  - Integrated image signal processor supports 13 MP up to 15fps
  - Supports electronic image stabilization
  - Supports video stabilization
  - Supports local contrast enhancement
  - Supports preference color adjustment
  - Supports noise reduction
  - Supports multiple frame noise reduction for video recording
  - Supports lens shading correction
  - Supports auto sensor defect pixel correction
  - Supports AE/AWB/AF
  - Supports edge enhancement (sharpness)
  - Supports face detection and visual tracking
  - Supports multiple frame blending for multi-motion special effect
  - Supports zero shutter delay image capture
  - Supports capturing full size image when recording video (up to 8M sensor)
  - Supports capturing stereo image without bridge IC
  - Supports stereo video recording without bridge IC
  - Supports MIPI CSI-2 high-speed camera serial interface with 4 data lane (for main) + 2 data lane (for stereo) + 2 data lane (for sub)
  - Supports Xenon flash

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  - Hardware JPEG decoder: Baseline decoding with 42M pixel/sec, progressive format decoding support
  - Hardware JPEG encoder: Baseline encoding with 90M pixel/sec
  - Supports YUV422/YUV420 color format and EXIF/JFIF format
  - Hardware WebP decoder

- **Video**
  - H.264 decoder: Baseline 1080p @ 30fps/40Mbps
  - H.264 decoder: Main/high profile 1080p@30fps/40Mbps
  - Sorenson H.263/H.263 decoder: 1080p @ 30fps/40Mbps
  - MPEG-4 SP/ASP decoder: 1080p @ 30fps/40Mbps
  - DIVX3/DIVX4/DIVX5/DIVX6/DIVX HD/XVID decoder: 1080p @ 30fps/40Mbps
  - VP8 decoder: 1080p @ 30fps/40Mbps
  - VC-1 decoder: 1080p @ 30fps/40Mbps
  - MPEG-4 encoder: Simple profile 1080p @ 30fps
  - H.263 encoder: 1080p @ 30fps
  - H.264 encoder: High profile 720p @ 30fps
  - VP8 encoder: 720p@ 30fps

- **Audio**
  - Sampling rates supported: 6kHz to 96kHz
  - Sample formats supported: 8-bit/16-bit, Mono/Stereo
  - Interfaces supported: DAI, I2S, PCM
  - 4-band IIR compensation filter to enhance loudspeaker responses
  - Proprietary audio post-processing technologies: BesLoudness, Android built-in post processing
  - Audio encode: AMR-NB, AMR-WB, AAC, OGG
  - Audio decode: WAV, MP3, MP2, AAC, AMR-NB, AMR-WB, MIDI, Vorbis, APE, AAC-plus v1, AAC-plus v2, FLAC, WMA

- **Speech**
  - Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR)
  - CTM
  - Noise reduction
  - Noise suppression
  - Noise cancellation
  - Dual-MIC noise cancellation
  - Echo cancellation
  - Echo suppression
  - Dual-MIC input
  - Digital MIC input

1.4 General Descriptions

MediaTek MT6589 is a highly integrated 3G System-on-chip (SoC) which incorporates advanced features e.g. HSPA R8 modem, Quad-core ARM® Cortex-A7 MPCore™ operating at 1.2 GHz, 3D graphics (OpenGL|ES 2.0), 13M camera ISP, LPDDR2 533MHz and high-definition 1080p video decoder. MT6589 helps phone manufacturers build high-performance 3G smart phones with PC-like browser, 3D gaming and cinema class home entertainment experiences.

World-leading technology

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Based on MediaTek's world-leading mobile chip SoC architecture with advanced 28nm process, MT6589 is the brand-new generation smart phone SoC integrating MediaTek HSPA R8 modem, 1.2GHz Quad-core ARM® Cortex-A7 MPCore™, 3D graphics and high-definition 1080p video decoder.

Rich in features, high-valued product

To enrich the camera features, MT6589 equips a 13M camera ISP with advanced features e.g. auto focus, anti-handshake, auto sensor defect pixel correction, continuous video AF, face detection, burst shot, optical zoom and panorama view.

Incredible browser experience

The 1.2GHz Quad-core ARM® Cortex-A7 MPCore™ with NEON multimedia processing engine brings PC-like browser experiences and helps accelerate OpenGL|ES 2.0 3D Adobe Flash 10 rendering performance to an unbeatable level.

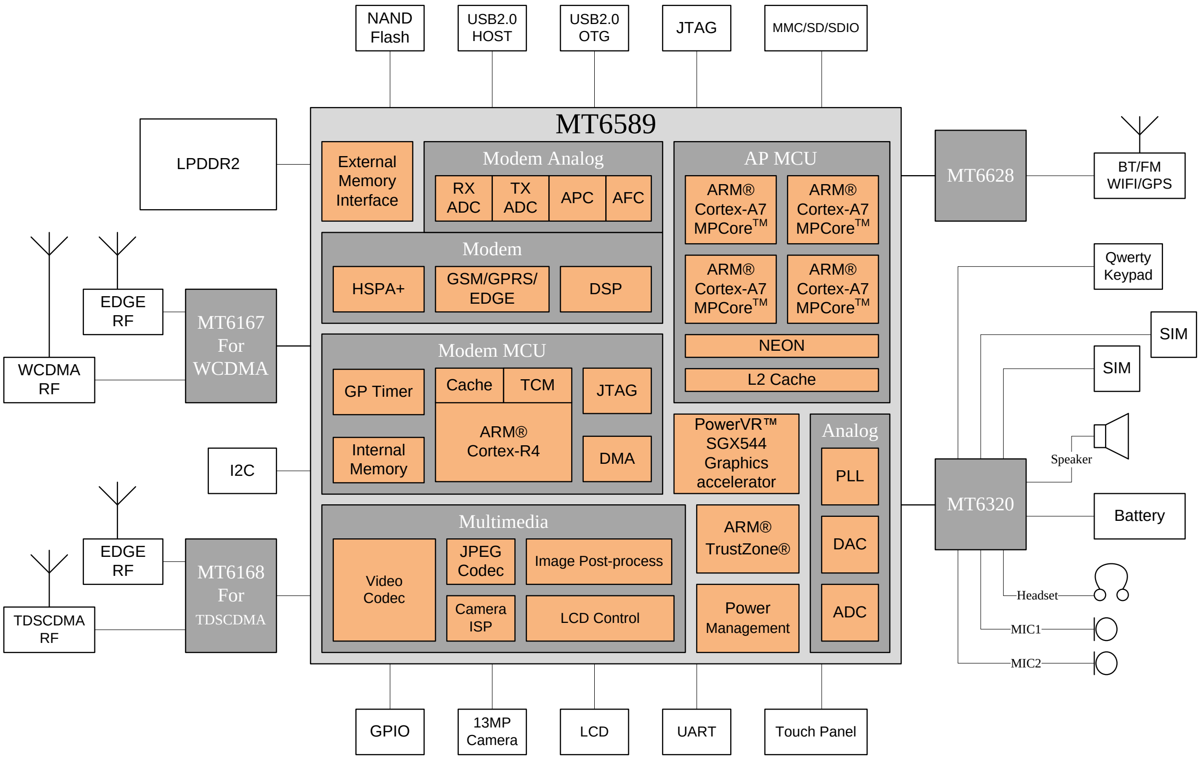

Figure 1-1: Block diagram of MT6589

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2 Product Description

2.1 Pin Description

2.1.1 Ball Map View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
A	NC	SCL2		MSDC3_DAT0	RDQ9			RDQM0	RDQ5			RDQ15	RA6		RA4		RDQ30			RDQ21	RDQM2			RDQ26	MSDC0_DAT4		MSDC0_DAT5	MSDC0_CMD	NC	A
B	SDA2	MRG_I2S_PCM_CLK	URXD3	MSDC3_DAT1	RDQ8		RDQ0	RDQ3	RDQ4		RDQ12	RDQ14	RA12	RBA0	RCAS_		RDQ31	RDQ28		RDQ20	RDQ18	RDQ16		RDQ25	MSDC0_DAT2	MSDC0_DAT0	MSDC0_DAT6	NLD4	NRNB	B
C	SDA1	MRG_I2S_PCM_RX	MRG_I2S_PCM_SYNC	MSDC3_CLK	GND	RDQ11	RDQ10	GND	RDQM1	RDQ6	RDQ13	RBA1		RRAS_	RODT	RA3	RA5	RDQM3	RDQ22	RDQ23	GND	RDQ24	RDQ27	GND		MSDC0_DAT1	MSDC0_CLK	NLD0	NLD7	C
D		SCL1	MSDC3_DAT3	MSDC3_DAT2	MSDC3_CMD	RDQ1	GND	RDQ2	GND	RDQ7	GND	RA14	RA1	RA10			RA13	GND	RDQ29	GND	RDQ19	GND	RDQ17	FSOURCE_P	MSDC0_DAT3	MSDC0_DAT7	NCLE	NLD14		D
E	DAI_RSTB	MRG_I2S_PCM_TX			SRCLKENAI	RDQS0			RDQS1_		RA8	RA11	RCKE	RCS_	REXTDN	RWE_	DDR3RSTB	RA0		RDQS3			RDQS2_		MSDC0_RSTB	NLD11		NLD8	NCEB0	E
F	DVDD18_NML4	CMPDN		UTXD3		RDQS0_			RDQS1			RCS1_				RA2	RA7	RA9		RDQS3_			RDQS2		NLD12			NLD13	NWEB	F
G		CMFLASH	CMMCLK	CMPCLK																					NLD15	NLD1	NLD3	NLD6		G
H	DVDD18_MIPIIO	CMRST	RDN0_B	RCN_B						DVDD18_EMI		RCLK1	RCLK1_	VREF	RCLK0_	RCLK0		VREF	DVDD18_EMI	DVDD18_EMI					NLD10	NALE	NLD2	NLD5	NCEB1	H
J	RDN1_B	RDP1_B	RDP0_B	RCP_B		GND				DVDD18_EMI	DVDD18_EMI			GND			DVDD18_EMI	DVDD18_EMI	DVDD18_EMI	DVDD18_EMI					NREB			NLD9	DVDD18_NML1	J
K		RDP1_A	RDN0_A	RCN_A		DVSS18_MIPIIO				GND	GND	GND	DVDD18_EMI		DVDD18_EMI	GND	GND	GND		DVDD18_EMI					ADC_CLK	ADC_WS		ADC_DAT_IN		K
L	RDP0	RDN1_A	RDP0_A	RCP_A			DVDD18_MIPIRX																	GND	TESTMODE	DAC_WS	DAC_DAT_OUT	PWRAP_EVENT	PWRAP_SPI0_CSN	L
M	RDN0	RDP2	RDN1	RCP		DVSS18_MIPIRX									AVSS18_MEMPLL	AVDD18_MEMPLL								SIM2_SCLK	SIM1_SIO	PWRAP_SPI0_MI	DAC_CLK	PWRAP_SPI0_MO	PWRAP_SPI0_CLK	M
N		RDN2	RDP1	RCN						DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	TN_MEMPLL	TP_MEMPLL					SIM2_SIO	SIM1_SCLK			SIM2_SRST		N
P	RDN3	RDP3	TDN0	TDP1		TDN3	TDP3	TCP		DVDD	GND	GND	GND	GND	GND	GND	DVDD	DVDD	DVDD	DVDD					RTC32K_CK	SRCLKENA		SIM1_SRST	SRCVOLTEN	P
R	TDP2	TDN2	TDP0	TDN1		VRT	TCN			GND	GND	DVDD_DVFS	GND	GND	DVDD_DVFS	GND	DVDD	GND	DVDD	GND				DVDD18_MC0	EINT4	IDDIG	EINT3	WATCHDOG	SYSRSTB	R
T		DVSS18_MIPITX	DVDD18_MIPITX	MSDC1_DAT1	MSDC1_DAT3			GND	GND	DVDD_GPU	GND	DVDD_DVFS	GND	GND	DVDD_DVFS	GND	DVDD	GND	DVDD	GND					JTRST_B	EINT2	EINT1	EINT0		T
U	DVDD33_MC1	MSDC1_CLK			MSDC1_CMD	MSDC1_SDWPI		GND	DVDD_GPU	DVDD_GPU	GND	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	GND	DVDD	GND	DVDD	DVDD				JTCK	JRTCK			JTDO	JTDI	U
V	MSDC1_DAT0	MSDC1_DAT2		MSDC2_DAT0	MSDC2_SDWPI	GND	GND	GND	DVDD_GPU	DVDD_GPU	GND	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	GND	DVDD	GND	GND	DVDD				UTXD2	UCTS2	JTMS		SDA3	SCL3	V
W		MSDC2_DAT2	MSDC2_CLK	MSDC2_CMD	MSDC2_DAT3			DVDD18_MC12			GND	DVDD_DVFS	DVDD_SRAM	DVDD_SRAM	DVDD_DVFS	GND			GND	DVDD				GND	URXD4	URXD2	PWM1	URTS2		W
Y	DVDD33_MC2	MSDC1_INSI	MSDC2_INSI	MSDC2_DAT1	DPIB4																			DVDD28_NML2	URTS1	URXD1	UTXD1	UTXD4	UCTS1	Y
AA	DPIB7	DPIG7			DPIG5	GND																			CHD_DM_P0	PWM3		PWM4	PWM2	AA
AB		DPIR2		DPIB3	DPIG1						VPROC_FB														CHD_DP_P0	AVSS33_USB_P0	USB_DM_P0	AVDD33_USB_P0		AB
AC	DPIG0	DPIHSYNC	DPIB0	DPIR6	DPIB1																					AVDD18_USB_P1	USB_DP_P0			AC
AD	DPIVSYNC	DPIR5	DPIG3	DPIB6	DPIR3	DPIG4		I2S_DATA_OUT		EINT10_AUXIN2	GND_VPROC_FB	AVSS18_AP				AVSS18_MD				GND				GND			AVDD18_USB_P0	USB_VRT	USB_DM_P1	AD
AE		DPIB5			DPIR0	LSA0	DISP_PWM	EINT5	SDA0	EINT11_AUXIN3	AUX_XM	AUX_YP	AVSS18_AP				AVSS18_MD			BSI1A_CS0	BSI1A_DATA1	BSI1B_DATA	BSI1B_CS0	BPI1_BUS18	DVDD28_BPI	BPI1_BUS16	USB_VBUS	AVSS33_USB_P1	USB_DP_P1	AE
AF	DVDD18_NML3	DPIR4		DPIDE	SPI1_MO	LPCE1B		EINT9	SCL0	EINT16_AUXIN4		AUX_XP	UL_Q_N2	UL_Q_P2	DL_Q_P2	DL_Q_N2	UL_I_N1	UL_I_P1	UL_Q_P1	UL_Q_N1	BSI1C_CLK	SRCLKENA2	BSI1B_CLK	BPI1_BUS11		BPI1_BUS6	BPI1_BUS4	VM0	AVDD33_USB_P1	AF
AG	DPIB2	DPIR7	DPIR1	LSCK	SPI1_CLK			EINT7	I2S_CLK			AUX_YM	UL_I_P2	UL_I_N2	DL_I_P2	DL_I_N2	DVDD18_MD	VBIAS	APC2	APC1		BSI1A_DATA2	DVDD28_BSI			BPI1_BUS1	BPI1_BUS8	BPI1_BUS5		AG
AH	DPIG2	DPIG6	LSDA	LPCE0B	SPI1_MI	LRSTB	LPTE	EINT6	I2S_WS	AUXIN1	AUXIN0	REFP	REFN	AVDD18_MD		DL_I_N1	DL_Q_N1	DL_Q_P1	AVDD28_DAC	TXBPI1	BSI1A_DATA0	BSI1A_CLK	BSI1C_DATA	BPI1_BUS10	BPI1_BUS13	BPI1_BUS9	BPI1_BUS17	BPI1_BUS3	VM1	AH
AJ	NC	DPICK	LSCE0B		LSCE1B	SPI1_CSN		EINT8	I2S_DATA_IN		DVDD18_PLLGP	AVDD18_AP		CLK26M2		DL_I_P1			CLK26M1		EXT_CLK_EN	DVDD18_BSI		BPI1_BUS0	BPI1_BUS7		BPI1_BUS2	BPI1_BUS12	NC	AJ
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	

Figure 2-1 : Ball map view of MT6589

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2.1.2 Pin Coordinate

Table 2-1: Pin coordinate

Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
A1	NC	K12	GND	W19	GND
A2	SCL2	K13	DVDD18_EMI	W20	DVDD
A4	MSDC3_DAT0	K15	DVDD18_EMI	W24	GND
A5	RDQ9	K16	GND	W25	URXD4
A8	RDQM0	K17	GND	W26	URXD2
A9	RDQ5	K18	GND	W27	PWM1
A12	RDQ15	K20	DVDD18_EMI	W28	URTS2
A13	RA6	K25	ADC_CLK	Y1	DVDD33_MC2
A15	RA4	K26	ADC_WS	Y2	MSDC1_INSI
A17	RDQ30	K28	ADC_DAT_IN	Y3	MSDC2_INSI
A20	RDQ21	L1	RDP0	Y4	MSDC2_DAT1
A21	RDQM2	L2	RDN1_A	Y5	DPIB4
A24	RDQ26	L3	RDP0_A	Y24	DVDD28_NML2
A25	MSDC0_DAT4	L4	RCP_A	Y25	URTS1
A27	MSDC0_DAT5	L7	DVDD18_MIPIRX	Y26	URXD1
A28	MSDC0_CMD	L24	GND	Y27	UTXD1
A29	NC	L25	TESTMODE	Y28	UTXD4
B1	SDA2	L26	DAC_WS	Y29	UCTS1
B2	MRG_I2S_PCM_CLK	L27	DAC_DAT_OUT	AA1	DPIB7
B3	URXD3	L28	PWRAP_EVENT	AA2	DPIG7
B4	MSDC3_DAT1	L29	PWRAP_SPI0_CSN	AA5	DPIG5
B5	RDQ8	M1	RDN0	AA6	GND
B7	RDQ0	M2	RDP2	AA25	CHD_DM_P0
B8	RDQ3	M3	RDN1	AA26	PWM3
B9	RDQ4	M4	RCP	AA28	PWM4
B11	RDQ12	M6	DVSS18_MIPIRX	AA29	PWM2
B12	RDQ14	M15	AVSS18_MEMPLL	AB2	DPIR2
B13	RA12	M16	AVDD18_MEMPLL	AB4	DPIB3
B14	RBA0	M24	SIM2_SCLK	AB5	DPIG1
B15	RCAS_	M25	SIM1_SIO	AB11	VPROC_FB
B17	RDQ31	M26	PWRAP_SPI0_MI	AB25	CHD_DP_P0
B18	RDQ28	M27	DAC_CLK	AB26	AVSS33_USB_P0
B20	RDQ20	M28	PWRAP_SPI0_MO	AB27	USB_DM_P0
B21	RDQ18	M29	PWRAP_SPI0_CLK	AB28	AVDD33_USB_P0
B22	RDQ16	N2	RDN2	AC1	DPIG0
B24	RDQ25	N3	RDP1	AC2	DPIHSYNC
B25	MSDC0_DAT2	N4	RCN	AC3	DPIB0
B26	MSDC0_DAT0	N10	DVDD	AC4	DPIR6
B27	MSDC0_DAT6	N11	DVDD	AC5	DPIB1
B28	NLD4	N12	DVDD	AC26	AVDD18_USB_P1
B29	NRNB	N13	DVDD	AC27	USB_DP_P0

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
C1	SDA1	N14	DVDD	AD1	DPIVSYNC
C2	MRG_I2S_PCM_RX	N15	DVDD	AD2	DPIR5
C3	MRG_I2S_PCM_SYNC	N16	DVDD	AD3	DPIG3
C4	MSDC3_CLK	N17	DVDD	AD4	DPIB6
C5	GND	N18	TN_MEMPLL	AD5	DPIR3
C6	RDQ11	N19	TP_MEMPLL	AD6	DPIG4
C7	RDQ10	N24	SIM2_SIO	AD8	I2S_DATA_OUT
C8	GND	N25	SIM1_SCLK	AD10	EINT10_AUXIN2
C9	RDQM1	N28	SIM2_SRST	AD11	GND_VPROC_FB
C10	RDQ6	P1	RDN3	AD12	AVSS18_AP
C11	RDQ13	P2	RDP3	AD16	AVSS18_MD
C12	RBA1	P3	TDN0	AD20	GND
C14	RRAS_	P4	TDP1	AD24	GND
C15	RODT	P6	TDN3	AD27	AVDD18_USB_P0
C16	RA3	P7	TDP3	AD28	USB_VRT
C17	RA5	P8	TCP	AD29	USB_DM_P1
C18	RDQM3	P10	DVDD	AE2	DPIB5
C19	RDQ22	P11	GND	AE5	DPIR0
C20	RDQ23	P12	GND	AE6	LSA0
C21	GND	P13	GND	AE7	DISP_PWM
C22	RDQ24	P14	GND	AE8	EINT5
C23	RDQ27	P15	GND	AE9	SDA0
C24	GND	P16	GND	AE10	EINT11_AUXIN3
C26	MSDC0_DAT1	P17	DVDD	AE11	AUX_XM
C27	MSDC0_CLK	P18	DVDD	AE12	AUX_YP
C28	NLD0	P19	DVDD	AE13	AVSS18_AP
C29	NLD7	P20	DVDD	AE17	AVSS18_MD
D2	SCL1	P25	RTC32K_CK	AE20	BSI1A_CS0
D3	MSDC3_DAT3	P26	SRCLKENA	AE21	BSI1A_DATA1
D4	MSDC3_DAT2	P28	SIM1_SRST	AE22	BSI1B_DATA
D5	MSDC3_CMD	P29	SRCVOLTEN	AE23	BSI1B_CS0
D6	RDQ1	R1	TDP2	AE24	BPI1_BUS18
D7	GND	R2	TDN2	AE25	DVDD28_BPI
D8	RDQ2	R3	TDP0	AE26	BPI1_BUS16
D9	GND	R4	TDN1	AE27	USB_VBUS
D10	RDQ7	R6	VRT	AE28	AVSS33_USB_P1
D11	GND	R7	TCN	AE29	USB_DP_P1
D12	RA14	R10	GND	AF1	DVDD18_NML3
D13	RA1	R11	GND	AF2	DPIR4
D14	RA10	R12	DVDD_DVFS	AF4	DPIDE
D17	RA13	R13	GND	AF5	SPI1_MO
D18	GND	R14	GND	AF6	LPCE1B
D19	RDQ29	R15	DVDD_DVFS	AF8	EINT9
D20	GND	R16	GND	AF9	SCL0

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
D21	RDQ19	R17	DVDD	AF10	EINT16_AUXIN4
D22	GND	R18	GND	AF12	AUX_XP
D23	RDQ17	R19	DVDD	AF13	UL_Q_N2
D24	FSOURCE_P	R20	GND	AF14	UL_Q_P2
D25	MSDC0_DAT3	R24	DVDD18_MC0	AF15	DL_Q_P2
D26	MSDC0_DAT7	R25	EINT4	AF16	DL_Q_N2
D27	NCLE	R26	IDDIG	AF17	UL_I_N1
D28	NLD14	R27	EINT3	AF18	UL_I_P1
E1	DAI_RSTB	R28	WATCHDOG	AF19	UL_Q_P1
E2	MRG_I2S_PCM_TX	R29	SYSRSTB	AF20	UL_Q_N1
E5	SRCLKENAI	T2	DVSS18_MIPITX	AF21	BSI1C_CLK
E6	RDQS0	T3	DVDD18_MIPITX	AF22	SRCLKENA2
E9	RDQS1_	T4	MSDC1_DAT1	AF23	BSI1B_CLK
E11	RA8	T5	MSDC1_DAT3	AF24	BPI1_BUS11
E12	RA11	T8	GND	AF26	BPI1_BUS6
E13	RCKE	T9	GND	AF27	BPI1_BUS4
E14	RCS_	T10	DVDD_GPU	AF28	VM0
E15	REXTDN	T11	GND	AF29	AVDD33_USB_P1
E16	RWE_	T12	DVDD_DVFS	AG1	DPIB2
E17	DDR3RSTB	T13	GND	AG2	DPIR7
E18	RA0	T14	GND	AG3	DPIR1
E20	RDQS3	T15	DVDD_DVFS	AG4	LSCK
E23	RDQS2_	T16	GND	AG5	SPI1_CLK
E25	MSDC0_RSTB	T17	DVDD	AG8	EINT7
E26	NLD11	T18	GND	AG9	I2S_CLK
E28	NLD8	T19	DVDD	AG12	AUX_YM
E29	NCEB0	T20	GND	AG13	UL_I_P2
F1	DVDD18_NML4	T25	JTRST_B	AG14	UL_I_N2
F2	CMPDN	T26	EINT2	AG15	DL_I_P2
F4	UTXD3	T27	EINT1	AG16	DL_I_N2
F6	RDQS0_	T28	EINT0	AG17	DVDD18_MD
F9	RDQS1	U1	DVDD33_MC1	AG18	VBIAS
F12	RCS1_	U2	MSDC1_CLK	AG19	APC2
F16	RA2	U5	MSDC1_CMD	AG20	APC1
F17	RA7	U6	MSDC1_SDWPI	AG22	BSI1A_DATA2
F18	RA9	U8	GND	AG23	DVDD28_BSI
F20	RDQS3_	U9	DVDD_GPU	AG26	BPI1_BUS1
F23	RDQS2	U10	DVDD_GPU	AG27	BPI1_BUS8
F25	NLD12	U11	GND	AG28	BPI1_BUS5
F28	NLD13	U12	DVDD_DVFS	AH1	DPIG2
F29	NWEB	U13	DVDD_DVFS	AH2	DPIG6
G2	CMFLASH	U14	DVDD_DVFS	AH3	LSDA
G3	CMMCLK	U15	DVDD_DVFS	AH4	LPCE0B
G4	CMPCLK	U16	GND	AH5	SPI1_MI

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
G25	NLD15	U17	DVDD	AH6	LRSTB
G26	NLD1	U18	GND	AH7	LPTE
G27	NLD3	U19	DVDD	AH8	EINT6
G28	NLD6	U20	DVDD	AH9	I2S_WS
H1	DVDD18_MIPIIO	U24	JTCK	AH10	AUXIN1
H2	CMRST	U25	JRTCK	AH11	AUXIN0
H3	RDN0_B	U28	JTDO	AH12	REFP
H4	RCN_B	U29	JTDI	AH13	REFN
H10	DVDD18_EMI	V1	MSDC1_DAT0	AH14	AVDD18_MD
H12	RCLK1	V2	MSDC1_DAT2	AH16	DL_I_N1
H13	RCLK1_	V4	MSDC2_DAT0	AH17	DL_Q_N1
H14	VREF	V5	MSDC2_SDWPI	AH18	DL_Q_P1
H15	RCLK0_	V6	GND	AH19	AVDD28_DAC
H16	RCLK0	V7	GND	AH20	TXBPI1
H18	VREF	V8	GND	AH21	BSI1A_DATA0
H19	DVDD18_EMI	V9	DVDD_GPU	AH22	BSI1A_CLK
H20	DVDD18_EMI	V10	DVDD_GPU	AH23	BSI1C_DATA
H25	NLD10	V11	GND	AH24	BPI1_BUS10
H26	NALE	V12	DVDD_DVFS	AH25	BPI1_BUS13
H27	NLD2	V13	DVDD_DVFS	AH26	BPI1_BUS9
H28	NLD5	V14	DVDD_DVFS	AH27	BPI1_BUS17
H29	NCEB1	V15	DVDD_DVFS	AH28	BPI1_BUS3
J1	RDN1_B	V16	GND	AH29	VM1
J2	RDP1_B	V17	DVDD	AJ1	NC
J3	RDP0_B	V18	GND	AJ2	DPICK
J4	RCP_B	V19	GND	AJ3	LSCE0B
J6	GND	V20	DVDD	AJ5	LSCE1B
J10	DVDD18_EMI	V24	UTXD2	AJ6	SPI1_CSN
J11	DVDD18_EMI	V25	UCTS2	AJ8	EINT8
J14	GND	V26	JTMS	AJ9	I2S_DATA_IN
J17	DVDD18_EMI	V28	SDA3	AJ11	DVDD18_PLLGP
J18	DVDD18_EMI	V29	SCL3	AJ12	AVDD18_AP
J19	DVDD18_EMI	W2	MSDC2_DAT2	AJ14	CLK26M2
J20	DVDD18_EMI	W3	MSDC2_CLK	AJ16	DL_I_P1
J25	NREB	W4	MSDC2_CMD	AJ19	CLK26M1
J28	NLD9	W5	MSDC2_DAT3	AJ21	EXT_CLK_EN
J29	DVDD18_NML1	W8	DVDD18_MC12	AJ22	DVDD18_BSI
K2	RDP1_A	W11	GND	AJ24	BPI1_BUS0
K3	RDN0_A	W12	DVDD_DVFS	AJ25	BPI1_BUS7
K4	RCN_A	W13	DVDD_SRAM	AJ27	BPI1_BUS2
K6	DVSS18_MIPIIO	W14	DVDD_SRAM	AJ28	BPI1_BUS12
K10	GND	W15	DVDD_DVFS	AJ29	NC
K11	GND	W16	GND		

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2.1.3 Detailed Pin Description

Table 2-2: Acronym for pin type

Abbreviation	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-direction
DI	Digital input
DO	Digital output
DIO	Digital bi-direction
P	Power
G	Ground

Table 2-3: Detailed pin description

Pin name	Type	Description	Power domain
SYSTEM			
SYSRSTB	DIO	System reset input	DVDD18_NML1
WATCHDOG	DO	Watchdog reset output	DVDD18_NML1
SRCVOLTEN	DIO	Wakeup signal to external PMIC	DVDD18_NML1
TESTMODE	DIO	Test mode	DVDD18_NML1
RTC32K_CK	DIO	32K clock intput	DVDD18_NML1
SRCLKENAI	DIO	26MHz co-clock enable input	DVDD18_NML4
SRCLKENA	DIO	26MHz co-clock enable output	DVDD18_NML1
PMIC			
PWRAP_SPI0_MO	DIO	PMIC SPI control interface	DVDD18_NML1
PWRAP_SPI0_MI	DIO	PMIC SPI control interface	DVDD18_NML1
PWRAP_SPI0_CSN	DIO	PMIC SPI control interface	DVDD18_NML1
PWRAP_SPI0_CLK	DIO	PMIC SPI control interface	DVDD18_NML1
PWRAP_EVENT	DIO	PMIC SPI control interface	DVDD18_NML1
ADC_CLK	DIO	PMIC audio input interface	DVDD18_NML1
ADC_WS	DIO	PMIC audio input interface	DVDD18_NML1
ADC_DAT_IN	DIO	PMIC audio input interface	DVDD18_NML1
DAC_CLK	DIO	PMIC audio output interface	DVDD18_NML1
DAC_WS	DIO	PMIC audio output interface	DVDD18_NML1
DAC_DAT_OUT	DIO	PMIC audio output interface	DVDD18_NML1
SIM			
SIM1_SIO	DIO	SIM1 data, PMIC interface	DVDD18_NML1
SIM1_SRST	DIO	SIM1 reset, PMIC interface	DVDD18_NML1
SIM1_SCLK	DIO	SIM1 clock, PMIC interface	DVDD18_NML1
SIM2_SIO	DIO	SIM2 data, PMIC interface	DVDD18_NML1
SIM2_SRST	DIO	SIM2 reset, PMIC interface	DVDD18_NML1
SIM2_SCLK	DIO	SIM2 clock, PMIC interface	DVDD18_NML1
JTAG			
JTCK	DIO	JTCK	DVDD18_NML1

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Pin name	Type	Description	Power domain
JTDO	DIO	JTDO	DVDD18_NML1
JTRST_B	DIO	JTRST_B	DVDD18_NML1
JTDI	DIO	JTDI	DVDD18_NML1
JRTCK	DIO	JRTCK	DVDD18_NML1
JTMS	DIO	JTMS	DVDD18_NML1
LCD			
DISP_PWM	DIO	Display PWM output	DVDD18_NML3
LPCE1B	DIO	Parallel display interface chip select 1 output	DVDD18_NML3
LPCE0B	DIO	Parallel display interface chip select 0 output	DVDD18_NML3
LPTE	DIO	Parallel display interface tearing effect	DVDD18_NML3
LRSTB	DIO	Parallel display interface Reset Signal	DVDD18_NML3
DPI			
DPIDE	DIO	Data enable signal of DPI	DVDD18_NML3
DPICK	DIO	Clock pin of DPI	DVDD18_NML3
DPIVSYNC	DIO	Vertical synchronization signal of DPI	DVDD18_NML3
DPIHSYNC	DIO	Horizontal synchronization signal of DPI	DVDD18_NML3
DPIR7	DIO	Data pin 7 of DPI R-channel/Data 23 for DBI parallel LCD interface	DVDD18_NML3
DPIR6	DIO	Data pin 6 of DPI R-channel/Data 22 for DBI parallel LCD interface	DVDD18_NML3
DPIR5	DIO	Data pin 5 of DPI R-channel/Data 21 for DBI parallel LCD interface	DVDD18_NML3
DPIR4	DIO	Data pin 4 of DPI R-channel/Data 20 for DBI parallel LCD interface	DVDD18_NML3
DPIR3	DIO	Data pin 3 of DPI R-channel/Data 19 for DBI parallel LCD interface	DVDD18_NML3
DPIR2	DIO	Data pin 2 of DPI R-channel/Data 18 for DBI parallel LCD interface	DVDD18_NML3
DPIR1	DIO	Data pin 1 of DPI R-channel/Data 17 for DBI parallel LCD interface	DVDD18_NML3
DPIR0	DIO	Data pin 0 of DPI R-channel/Data 16 for DBI parallel LCD interface	DVDD18_NML3
DPIG7	DIO	Data pin 7 of DPI G-channel/Data 15 for DBI parallel LCD interface	DVDD18_NML3
DPIG6	DIO	Data pin 6 of DPI G-channel/Data 14 for DBI parallel	DVDD18_NML3

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Pin name	Type	Description	Power domain
		LCD interface	
DPIG5	DIO	Data pin 5 of DPI G-channel/Data 13 for DBI parallel LCD interface	DVDD18_NML3
DPIG4	DIO	Data pin 4 of DPI G-channel/Data 12 for DBI parallel LCD interface	DVDD18_NML3
DPIG3	DIO	Data pin 3 of DPI G-channel/Data 11 for DBI parallel LCD interface	DVDD18_NML3
DPIG2	DIO	Data pin 2 of DPI G-channel/Data 10 for DBI parallel LCD interface	DVDD18_NML3
DPIG1	DIO	Data pin 1 of DPI G-channel/Data 9 for DBI parallel LCD interface	DVDD18_NML3
DPIG0	DIO	Data pin 0 of DPI G-channel/Data 8 for DBI parallel LCD interface	DVDD18_NML3
DPIB7	DIO	Data pin 7 of DPI B-channel/Data 7 for DBI parallel LCD interface	DVDD18_NML3
DPIB6	DIO	Data pin 6 of DPI B-channel/Data 6 for DBI parallel LCD interface	DVDD18_NML3
DPIB5	DIO	Data pin 5 of DPI B-channel/Data 5 for DBI parallel LCD interface	DVDD18_NML3
DPIB4	DIO	Data pin 4 of DPI B-channel/Data 4 for DBI parallel LCD interface	DVDD18_NML3
DPIB3	DIO	Data pin 3 of DPI B-channel/Data 3 for DBI parallel LCD interface	DVDD18_NML3
DPIB2	DIO	Data pin 2 of DPI B-channel/Data 2 for DBI parallel LCD interface	DVDD18_NML3
DPIB1	DIO	Data pin 1 of DPI B-channel/Data 1 for DBI parallel LCD interface	DVDD18_NML3
DPIB0	DIO	Data pin 0 of DPI B-channel/Data 0 for DBI parallel LCD interface	DVDD18_NML3
SLCD			
LSCE0B	DIO	Serial display interface chip select 0 output	DVDD18_NML3
LSCK	DIO	Serial display interface clock output	DVDD18_NML3
LSCE1B	DIO	Serial display interface chip select 1 output	DVDD18_NML3
LSDA	DIO	Serial display interface data	DVDD18_NML3
LSA0	DIO	Serial display interface address	DVDD18_NML3

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Pin name	Type	Description	Power domain
		output	
I2S			
I2S_DATA_IN	DIO	I2S data input pin	DVDD18_NML3
I2S_DATA_OUT	DIO	I2S data output pin	DVDD18_NML3
I2S_WS	DIO	I2S word select	DVDD18_NML3
I2S_CK	DIO	I2S clock	DVDD18_NML3
PCM/I2S merge interface			
MRG_I2S_PCM_TX	DIO	PCM/I2S/merge audio interface to MT6628	DVDD18_NML4
MRG_I2S_PCM_CLK	DIO	PCM/I2S/merge audio interface to MT6628	DVDD18_NML4
MRG_I2S_PCM_RX	DIO	PCM/I2S/merge audio interface to MT6628	DVDD18_NML4
MRG_I2S_PCM_SYNC	DIO	PCM/I2S/merge audio interface to MT6628	DVDD18_NML4
DAI_RSTB	DIO	PCM/I2S/merge audio interface to MT6628	DVDD18_NML4
EINT			
EINT0	DIO	External interrupt 0	DVDD18_NML1
EINT1	DIO	External interrupt 1	DVDD18_NML1
EINT2	DIO	External interrupt 2	DVDD18_NML1
EINT3	DIO	External interrupt 3	DVDD18_NML1
EINT4	DIO	External interrupt 4	DVDD18_NML1
EINT5	DIO	External interrupt 5	DVDD18_NML3
EINT6	DIO	External interrupt 6	DVDD18_NML3
EINT7	DIO	External interrupt 7	DVDD18_NML3
EINT8	DIO	External interrupt 8	DVDD18_NML3
EINT9	DIO	External interrupt 9	DVDD18_NML3
EINT10_AUX_IN2	DIO/AIO	External interrupt 10/Aux ADC external channel 2	DVDD18_NML3
EINT11_AUX_IN3	DIO/AIO	External interrupt 11/Aux ADC external channel 3	DVDD18_NML3
EINT16_AUX_IN4	DIO/AIO	External interrupt 16/Aux ADC external channel 4	DVDD18_NML3
PWM			
PWM1	DIO	PWM1	DVDD28_NML2
PWM2	DIO	PWM2	DVDD28_NML2
PWM3	DIO	PWM3	DVDD28_NML2
PWM4	DIO	PWM4	DVDD28_NML2
UART1			
URXD1	DIO	UART1 RX	DVDD28_NML2
URTS1	DIO	UART1 RTS	DVDD28_NML2
UCTS1	DIO	UART1 CTS	DVDD28_NML2
UTXD1	DIO	UART1 TX	DVDD28_NML2
UART2			
UTXD2	DIO	UART2 TX	DVDD18_NML1
URXD2	DIO	UART2 RX	DVDD18_NML1

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Pin name	Type	Description	Power domain
UCTS2	DIO	UART2 CTS	DVDD18_NML1
URTS2	DIO	UART2 RTS	DVDD18_NML1
UART3			
UTXD3	DIO	UART3 TX	DVDD18_NML4
URXD3	DIO	UART3 RX	DVDD18_NML4
UART4			
UTXD4	DIO	UART4 TX	DVDD28_NML2
URXD4	DIO	UART4 RX	DVDD28_NML2
SPI			
SPI1_CSN	DIO	SPI1 chip select	DVDD18_NML3
SPI1_MI	DIO	SPI1 data in	DVDD18_NML3
SPI1_MO	DIO	SPI1 data out	DVDD18_NML3
SPI1_CLK	DIO	SPI1 clock	DVDD18_NML3
BPI			
BPI_BUS0	DIO	BPI BUS0	DVDD28_BPI
BPI_BUS1	DIO	BPI BUS1	DVDD28_BPI
BPI_BUS2	DIO	BPI BUS2	DVDD28_BPI
BPI_BUS3	DIO	BPI BUS3	DVDD28_BPI
BPI_BUS4	DIO	BPI BUS4	DVDD28_BPI
BPI_BUS5	DIO	BPI BUS5	DVDD28_BPI
BPI_BUS6	DIO	BPI BUS6	DVDD28_BPI
BPI_BUS7	DIO	BPI BUS7	DVDD28_BPI
BPI_BUS8	DIO	BPI BUS8	DVDD28_BPI
BPI_BUS9	DIO	BPI BUS9	DVDD28_BPI
BPI_BUS10	DIO	BPI BUS10	DVDD28_BPI
BPI_BUS11	DIO	BPI BUS11	DVDD28_BPI
BPI_BUS12	DIO	BPI BUS12	DVDD28_BPI
BPI_BUS13	DIO	BPI BUS13	DVDD28_BPI
BPI_BUS16	DIO	BPI BUS16	DVDD28_BPI
BPI_BUS17	DIO	BPI BUS17	DVDD28_BPI
BPI_BUS18	DIO	BPI BUS18	DVDD28_BPI
VM			
VM1	DIO	PA mode selection	DVDD28_BPI
VM0	DIO	PA mode selection	DVDD28_BPI
BSI			
BSI1A_CS0	DIO	BSI1A CS0	DVDD18_BSI
BSI1A_CLK	DIO	BSI1A CLK	DVDD18_BSI
BSI1A_DATA0	DIO	BSI1A DATA0	DVDD18_BSI
BSI1A_DATA1	DIO	BSI1A DATA1	DVDD18_BSI
BSI1A_DATA2	DIO	BSI1A DATA2	DVDD18_BSI
BSI1B_CS0	DIO	BSI1B CS0	DVDD28_BSI
BSI1B_CLK	DIO	BSI1B CLK	DVDD28_BSI
BSI1B_DATA	DIO	BSI1B DATA	DVDD28_BSI
BSI1C_CLK	DIO	BSI1C CLK	DVDD18_BSI
BSI1C_DATA	DIO	BSI1C DATA	DVDD18_BSI

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Pin name	Type	Description	Power domain
TXBPI1	DIO	RF MT6167 TXBPI1	DVDD18_BSI
EXT_CLK_EN	DIO	Co-clock control pin	DVDD18_BSI
SRCLKENA2	DIO	Co-clock control pin	DVDD18_BSI
MSDC0			
MSDC0_DAT6	DIO	MSDC0 data6 pin	DVDD18_MC0
MSDC0_DAT7	DIO	MSDC0 data7 pin	DVDD18_MC0
MSDC0_DAT5	DIO	MSDC0 data5 pin	DVDD18_MC0
MSDC0_RSTB	DIO	MSDC0 reset output	DVDD18_MC0
MSDC0_DAT4	DIO	MSDC0 data4 pin	DVDD18_MC0
MSDC0_DAT2	DIO	MSDC0 data2 pin	DVDD18_MC0
MSDC0_DAT3	DIO	MSDC0 data3 pin	DVDD18_MC0
MSDC0_CMD	DIO	MSDC0 command pin	DVDD18_MC0
MSDC0_CLK	DIO	MSDC0 clock output	DVDD18_MC0
MSDC0_DAT1	DIO	MSDC0 data1 pin	DVDD18_MC0
MSDC0_DAT0	DIO	MSDC0 data0 pin	DVDD18_MC0
MSDC1			
MSDC1_CLK	DIO	MSDC1 clock output	DVDD33_MC1/DVDD18_MC12
MSDC1_CMD	DIO	MSDC1 command pin	DVDD33_MC1/DVDD18_MC12
MSDC1_DAT0	DIO	MSDC1 data0 pin	DVDD33_MC1/DVDD18_MC12
MSDC1_DAT1	DIO	MSDC1 data1 pin	DVDD33_MC1/DVDD18_MC12
MSDC1_DAT2	DIO	MSDC1 data2 pin	DVDD33_MC1/DVDD18_MC12
MSDC1_DAT3	DIO	MSDC1 data3 pin	DVDD33_MC1/DVDD18_MC12
MSDC1_SDWPI	DIO	MSDC1 WP pin	DVDD33_MC1/DVDD18_MC12
MSDC1_INSI	DIO	MSDC1 card insertion	DVDD18_NML3
MSDC2			
MSDC2_CLK	DIO	MSDC2 clock output	DVDD33_MC2/DVDD18_MC12
MSDC2_CMD	DIO	MSDC2 command pin	DVDD33_MC2/DVDD18_MC12
MSDC2_DAT0	DIO	MSDC2 data0 pin	DVDD33_MC2/DVDD18_MC12
MSDC2_DAT1	DIO	MSDC2 data1 pin	DVDD33_MC2/DVDD18_MC12
MSDC2_DAT2	DIO	MSDC2 data2 pin	DVDD33_MC2/DVDD18_MC12
MSDC2_DAT3	DIO	MSDC2 data3 pin	DVDD33_MC2/DVDD18_MC12
MSDC2_SDWPI	DIO	MSDC2 WP pin	DVDD33_MC2/DVDD18_MC12
MSDC2_INSI	DIO	MSDC2 card insertion	DVDD33_MC2/DVDD18_MC12
MSDC3			
MSDC3_CLK	DIO	MSDC3 clock output	DVDD18_NML4
MSDC3_CMD	DIO	MSDC3 command pin	DVDD18_NML4
MSDC3_DAT0	DIO	MSDC3 data0 pin	DVDD18_NML4
MSDC3_DAT1	DIO	MSDC3 data1 pin	DVDD18_NML4
MSDC3_DAT2	DIO	MSDC3 data2 pin	DVDD18_NML4
MSDC3_DAT3	DIO	MSDC3 data3 pin	DVDD18_NML4
NFI			
NCEB0	DIO	Parallel NAND interface chip select 0 output	DVDD18_NML1
NCEB1	DIO	Parallel NAND interface chip select 1 output	DVDD18_NML1

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Pin name	Type	Description	Power domain
NRNB	DIO	Parallel NAND interface chip ready input	DVDD18_NML1
NCLE	DIO	Parallel NAND interface command latch enable output	DVDD18_NML1
NALE	DIO	Parallel NAND interface address latch enable output	DVDD18_NML1
NREB	DIO	Parallel NAND interface read strobe output	DVDD18_NML1
NWEB	DIO	Parallel NAND interface write strobe output	DVDD18_NML1
NLD0	DIO	Nand-Flash Data 0	DVDD18_NML1
NLD1	DIO	Nand-Flash Data 1	DVDD18_NML1
NLD2	DIO	Nand-Flash Data 2	DVDD18_NML1
NLD3	DIO	Nand-Flash Data 3	DVDD18_NML1
NLD4	DIO	Nand-Flash Data 4	DVDD18_NML1
NLD5	DIO	Nand-Flash Data 5	DVDD18_NML1
NLD6	DIO	Nand-Flash Data 6	DVDD18_NML1
NLD7	DIO	Nand-Flash Data 7	DVDD18_NML1
NLD8	DIO	Nand-Flash Data 8	DVDD18_NML1
NLD9	DIO	Nand-Flash Data 9	DVDD18_NML1
NLD10	DIO	Nand-Flash Data 10	DVDD18_NML1
NLD11	DIO	Nand-Flash Data 11	DVDD18_NML1
NLD12	DIO	Nand-Flash Data 12	DVDD18_NML1
NLD13	DIO	Nand-Flash Data 13	DVDD18_NML1
NLD14	DIO	Nand-Flash Data 14	DVDD18_NML1
NLD15	DIO	Nand-Flash Data 15	DVDD18_NML1
EFUSE			
FSOURCE_P	DIO	E-FUSE blowing power control	FSOURCE_P
EMI			
DDR3RSTB	DIO	DDR3 reset output #	DVDD18_EMI
RCLK0	DIO	DRAM clock 0 output	DVDD18_EMI
RCLK0_	DIO	DRAM clock 0 output #	DVDD18_EMI
RCLK1	DIO	DRAM clock 1 output	DVDD18_EMI
RCLK1_	DIO	DRAM clock 1 output #	DVDD18_EMI
RCKE	DIO	DRAM command output CKE	DVDD18_EMI
RCS_	DIO	DRAM chip select 0 #	DVDD18_EMI
RCS1_	DIO	DRAM chip select 1 #	DVDD18_EMI
RCAS_	DIO	DRAM command output CAS#	DVDD18_EMI
RRAS_	DIO	DRAM command output RAS#	DVDD18_EMI
RWE_	DIO	DRAM command output WR#	DVDD18_EMI
RBA0	DIO	DRAM bank address output 0	DVDD18_EMI
RBA1	DIO	DRAM bank address output 1	DVDD18_EMI
RA0	DIO	DRAM address output 0	DVDD18_EMI
RA1	DIO	DRAM address output 1	DVDD18_EMI
RA2	DIO	DRAM address output 2	DVDD18_EMI
RA3	DIO	DRAM address output 3	DVDD18_EMI

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Pin name	Type	Description	Power domain
RA4	DIO	DRAM address output 4	DVDD18_EMI
RA5	DIO	DRAM address output 5	DVDD18_EMI
RA6	DIO	DRAM address output 6	DVDD18_EMI
RA7	DIO	DRAM address output 7	DVDD18_EMI
RA8	DIO	DRAM address output 8	DVDD18_EMI
RA9	DIO	DRAM address output 9	DVDD18_EMI
RA10	DIO	DRAM address output 10	DVDD18_EMI
RA11	DIO	DRAM address output 11	DVDD18_EMI
RA12	DIO	DRAM address output 12	DVDD18_EMI
RA13	DIO	DRAM address output 13	DVDD18_EMI
RA14	DIO	DRAM address output 14	DVDD18_EMI
RDQM0	DIO	DRAM DQM 0	DVDD18_EMI
RDQM1	DIO	DRAM DQM 1	DVDD18_EMI
RDQM2	DIO	DRAM DQM 2	DVDD18_EMI
RDQM3	DIO	DRAM DQM 3	DVDD18_EMI
RDQS0	DIO	DRAM DQS 0	DVDD18_EMI
RDQS0_	DIO	DRAM DQS 0 #	DVDD18_EMI
RDQS1	DIO	DRAM DQS 1	DVDD18_EMI
RDQS1_	DIO	DRAM DQS 1 #	DVDD18_EMI
RDQS2	DIO	DRAM DQS 2	DVDD18_EMI
RDQS2_	DIO	DRAM DQS 2 #	DVDD18_EMI
RDQS3	DIO	DRAM DQS 3	DVDD18_EMI
RDQS3_	DIO	DRAM DQS 3 #	DVDD18_EMI
RDQ0	DIO	DRAM data pin 0	DVDD18_EMI
RDQ1	DIO	DRAM data pin 1	DVDD18_EMI
RDQ2	DIO	DRAM data pin 2	DVDD18_EMI
RDQ3	DIO	DRAM data pin 3	DVDD18_EMI
RDQ4	DIO	DRAM data pin 4	DVDD18_EMI
RDQ5	DIO	DRAM data pin 5	DVDD18_EMI
RDQ6	DIO	DRAM data pin 6	DVDD18_EMI
RDQ7	DIO	DRAM data pin 7	DVDD18_EMI
RDQ8	DIO	DRAM data pin 8	DVDD18_EMI
RDQ9	DIO	DRAM data pin 9	DVDD18_EMI
RDQ10	DIO	DRAM data pin 10	DVDD18_EMI
RDQ11	DIO	DRAM data pin 11	DVDD18_EMI
RDQ12	DIO	DRAM data pin 12	DVDD18_EMI
RDQ13	DIO	DRAM data pin 13	DVDD18_EMI
RDQ14	DIO	DRAM data pin 14	DVDD18_EMI
RDQ15	DIO	DRAM data pin 15	DVDD18_EMI
RDQ16	DIO	DRAM data pin 16	DVDD18_EMI
RDQ17	DIO	DRAM data pin 17	DVDD18_EMI
RDQ18	DIO	DRAM data pin 18	DVDD18_EMI
RDQ19	DIO	DRAM data pin 19	DVDD18_EMI
RDQ20	DIO	DRAM data pin 20	DVDD18_EMI
RDQ21	DIO	DRAM data pin 21	DVDD18_EMI

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Pin name	Type	Description	Power domain
RDQ22	DIO	DRAM data pin 22	DVDD18_EMI
RDQ23	DIO	DRAM data pin 23	DVDD18_EMI
RDQ24	DIO	DRAM data pin 24	DVDD18_EMI
RDQ25	DIO	DRAM data pin 25	DVDD18_EMI
RDQ26	DIO	DRAM data pin 26	DVDD18_EMI
RDQ27	DIO	DRAM data pin 27	DVDD18_EMI
RDQ28	DIO	DRAM data pin 28	DVDD18_EMI
RDQ29	DIO	DRAM data pin 29	DVDD18_EMI
RDQ30	DIO	DRAM data pin 30	DVDD18_EMI
RDQ31	DIO	DRAM data pin 31	DVDD18_EMI
RODT(/RBA2)	DIO	DRAM ODT pin(/DRAM bank address output 2)	DVDD18_EMI
REXTDN	DIO	DRAM REXTDN pin	DVDD18_EMI
CAM			
CMPCLK	DIO	Pixel clock from sensor	DVDD18_NML4
CMMCLK	DIO	Master clock to sensor	DVDD18_NML4
CMRST	DIO	Reset control to sensor	DVDD18_NML4
CMPDN	DIO	Power down to sensor	DVDD18_NML4
CMFLASH	DIO	Camera flash control signal	DVDD18_NML4
I2C0			
SCL0	DIO	I2C0 clock	DVDD18_NML3
SDA0	DIO	I2C0 data	DVDD18_NML3
I2C1			
SCL1	DIO	I2C1 clock	DVDD18_NML4
SDA1	DIO	I2C1 data	DVDD18_NML4
I2C2			
SCL2	DIO	I2C2 clock	DVDD18_NML4
SDA2	DIO	I2C2 data	DVDD18_NML4
I2C3			
SCL3	DIO	I2C3 clock	DVDD18_NML1
SDA3	DIO	I2C3 data	DVDD18_NML1
ABB			
UL_Q_N1	AIO	UMTS uplink for UMTSTX_QN	DVDD18_MD
UL_Q_P1	AIO	UMTS uplink for UMTSTX_QP	DVDD18_MD
UL_I_P1	AIO	UMTS uplink for UMTSTX_IP	DVDD18_MD
UL_I_N1	AIO	UMTS uplink for UMTSTX_IN	DVDD18_MD
VBIAS	AIO	3G PA analog control	AVDD28_DAC
APC1	AIO	Automatic power control for 1st modem	AVDD28_DAC
APC2	AIO	Automatic power control for 2nd modem	AVDD28_DAC
CLK26M1	AIO	26MHz clock input for AP & 1st modem	AVDD18_MD
DL_Q_P1	AIO	UMTS uplink for UMTSRX_QP	DVDD18_MD
DL_Q_N1	AIO	UMTS uplink for UMTSRX_QN	DVDD18_MD
DL_I_N1	AIO	UMTS uplink for UMTSRX_IN	DVDD18_MD

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Pin name	Type	Description	Power domain
DL_I_P1	AIO	UMTS uplink for UMTSRX_IP	DVDD18_MD
DL_Q_P2	AIO	UMTS uplink for 2nd UMTSRX_QP or WCDMA diversity path	DVDD18_MD
DL_Q_N2	AIO	UMTS uplink for 2nd UMTSRX_QN or WCDMA diversity path	DVDD18_MD
DL_I_N2	AIO	UMTS uplink for 2nd UMTSRX_IN or WCDMA diversity path	DVDD18_MD
DL_I_P2	AIO	UMTS uplink for 2nd UMTSRX_IP or WCDMA diversity path	DVDD18_MD
CLK26M2	AIO	26MHz clock input for AP & 2nd modem	AVDD18_MD
UL_Q_N2	AIO	UMTS uplink for 2nd UMTSTX_QN	AVDD18_MD
UL_Q_P2	AIO	UMTS uplink for 2nd UMTSTX_QP	AVDD18_MD
UL_I_P2	AIO	UMTS uplink for 2nd UMTSTX_IP	AVDD18_MD
UL_I_N2	AIO	UMTS uplink for 2nd UMTSTX_IN	AVDD18_MD
REFN	AIO	Negative reference port for internal circuit	AVDD18_AP
REFP	AIO	Positive reference port for internal circuit	AVDD18_AP
AUX_IN0	AIO	AuxADC external input channel 0	AVDD18_AP
AUX_IN1	AIO	AuxADC external input channel 1	AVDD18_AP
AUX_XP	AIO	AuxADC channel for touch screen TP_X+	AVDD18_AP
AUX_YP	AIO	AuxADC channel for touch screen TP_Y+	AVDD18_AP
AUX_XM	AIO	AuxADC channel for touch screen TP_X-	AVDD18_AP
AUX_YM	AIO	AuxADC channel for touch screen TP_Y-	AVDD18_AP
MIPI			
TDN3	AIO	DSI0 lane3 N	DVDD18_MIPITX
TDP3	AIO	DSI0 lane3 P	DVDD18_MIPITX
TDN2	AIO	DSI0 lane2 N	DVDD18_MIPITX
TDP2	AIO	DSI0 lane2 P	DVDD18_MIPITX
TCN	AIO	DSI0 CK lane N	DVDD18_MIPITX
TCP	AIO	DSI0 CK lane P	DVDD18_MIPITX
TDN1	AIO	DSI0 lane1 N	DVDD18_MIPITX
TDP1	AIO	DSI0 lane1 P	DVDD18_MIPITX
TDN0	AIO	DSI0 lane0 N	DVDD18_MIPITX
TDP0	AIO	DSI0 lane0 P	DVDD18_MIPITX

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Pin name	Type	Description	Power domain
VRT	AO	External resistor for DSI bias Connect 1.5K ohm 1% resistor to ground.	DVDD18_MIPITX
RDN3	AIO	CSI0 lane3 N	DVDD18_MIPIRX
RDP3	AIO	CSI0 lane3 P	DVDD18_MIPIRX
RDN2	AIO	CSI0 lane2 N	DVDD18_MIPIRX
RDP2	AIO	CSI0 lane2 P	DVDD18_MIPIRX
RCN	AIO	CSI0 CK lane N	DVDD18_MIPIRX
RCP	AIO	CSI0 CK lane P	DVDD18_MIPIRX
RDN1	AIO	CSI0 lane1 N	DVDD18_MIPIRX
RDP1	AIO	CSI0 lane1 P	DVDD18_MIPIRX
RDN0	AIO	CSI0 lane0 N	DVDD18_MIPIRX
RDP0	AIO	CSI0 lane0 P	DVDD18_MIPIRX
RDN1_A	AIO	CSI1 lane1 N/Pixel data [6] from sensor	DVDD18_MIPIIO
RDP1_A	AIO	CSI1 lane1 P/Pixel data [7] from sensor	DVDD18_MIPIIO
RCN_A	AIO	CSI1 CK lane N/Pixel data [8] from sensor	DVDD18_MIPIIO
RCP_A	AIO	CSI1 CK lane P/Pixel data [9] from sensor	DVDD18_MIPIIO
RDN0_A	AIO	CSI1 lane0 N/VREF from sensor	DVDD18_MIPIIO
RDP0_A	AIO	CSI1 lane0 P/HREF from sensor	DVDD18_MIPIIO
RDN1_B	AIO	CSI1 sub-cam lane1 N/Pixel data [2] from sensor	DVDD18_MIPIIO
RDP1_B	AIO	CSI1 sub-cam lane1 P/Pixel data [3] from sensor	DVDD18_MIPIIO
RCN_B	AIO	CSI1 sub-cam CK lane N/Pixel data [4] from sensor	DVDD18_MIPIIO
RCP_B	AIO	CSI1 sub-cam CK lane P/Pixel data [5] from sensor	DVDD18_MIPIIO
RDN0_B	AIO	CSI1 sub-cam lane0 N/Pixel data [0] from sensor	DVDD18_MIPIIO
RDP0_B	AIO	CSI1 sub-cam lane0 P/Pixel data [1] from sensor	DVDD18_MIPIIO
USB			
USB_DP_P0	AIO	USB port0 D+ differential data line	AVDD33_USB_P0
USB_DM_P0	AIO	USB port0 D- differential data line	AVDD33_USB_P0
CHD_DP_P0	AIO	BC1.1 Charger DP	AVDD33_USB_P0
CHD_DM_P0	AIO	BC1.1 Charger DM	AVDD33_USB_P0
USB_VRT	AO	USB output for bias current; connect with 5.11K 1% Ohm to GND	AVDD18_USB_P0
USB_VBUS	AI	Power for connected device +3.3V	AVDD18_USB_P0

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Pin name	Type	Description	Power domain
USB_DP_P1	AIO	USB port1 D+ differential data line	AVDD33_USB_P1
USB_DM_P1	AIO	USB port1 D- differential data line	AVDD33_USB_P1
IDDIG	DIO	USB OTG ID pin	DVDD18_NML1
MEMPLL			
TP_MEMPLL	AIO	MEMPLL differential output P for debug	AVDD18_MEMPLL
TN_MEMPLL	AIO	MEMPLL differential output N for debug	AVDD18_MEMPLL
Analog power			
DVDD18_PLLGP	P	Analog power input 1.8V for PLL	
AVDD18_AP	P	Analog power input 1.8V for AuxADC, TSENSE	
AVDD18_MD	P	Analog power input 1.8V for BBTX, BBRX, 2GBBTX	
DVDD18_MD	P	Alternative analog power input 1.8V for BBTX, BBRX, 2GBBTX	
AVDD28_DAC	P	Analog power input 2.8V for APC	
DVDD18_MIPITX	P	Analog power for MIPI DSI	
DVDD18_MIPIRX	P	Analog power for MIPI CSI0	
DVDD18_MIPIIO	P	Analog power for MIPI CSI1 & GPI	
AVDD33_USB_P0	P	Analog power 3.3V for USB port 0	
AVDD33_USB_P1	P	Analog power 3.3V for USB port 1	
AVDD18_USB_P0	P	Analog power 1.8V for USB port 0	
AVDD18_USB_P1	P	Analog power 1.8V for USB port 1	
AVDD18_MEMPLL	P	Analog power for MEMPLL	
Digital power			
DVDD18_NML1	P	Digital power input for NML1	-
DVDD28_NML2	P	Digital power input for NML2	-
DVDD18_NML3	P	Digital power input for NML3	-
DVDD18_NML4	P	Digital power input for NML4	-
DVDD28_BPI	P	Digital power input for 2.8V BPI IO	-
DVDD28_BSI	P	Digital power input for 2.8V BSI IO	-
DVDD18_BSI	P	Digital power input for 1.8V BSI IO	-
DVDD18_EMI	P	Digital power input for EMI	-
DVDD18_MC0	P	Digital power input for MSDC0	-
DVDD33_MC1	P	Digital power input for MSDC1 transmitter	-

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Pin name	Type	Description	Power domain
DVDD33_MC2	P	Digital power input for MSDC2 transmitter	-
DVDD18_MC12	P	Digital power input for MSDC1/MSDC2 receiver	-
DVDD_GPU	P	Digital power input for graphic processor	-
DVDD	P	Digital power input for core	-
DVDD_DVFS	P	Digital power input for processor	-
DVDD_SRAM	P	Digital power input for processor memory	-
Analog ground			
AVSS18_AP	G		
AVSS18_MD	G		
DVSS18_MIPITX	G		
DVSS18_MIPIRX	G		
DVSS18_MIPIIO	G		
AVSS33_USB_P0	G		
AVSS33_USB_P1	G		
AVSS18_MEMPLL	G		
Digital ground			
GND	G		-

2.2 Electrical Characteristic

2.2.1 Absolute Maximum Ratings

Table 2-4: Absolute maximum ratings for power supply

Symbol or pin name	Description	Min.	Max.	Unit
DVDD18_PLLGP	Analog power input 1.8V for PLL	1.7	1.9	V
AVDD18_AP	Analog power input 1.8V for AuxADC, TSENSE	1.7	1.9	V
AVDD18_MD	Analog power input 1.8V for BBTX, BBRX, 2GBBTX	1.7	1.9	V
DVDD18_MD	Alternative analog power input 1.8V for BBTX, BBRX, 2GBBTX	1.7	1.9	V
AVDD28_DAC	Analog power input 2.8V for APC	2.66	2.94	V
DVDD18_MIPITX	Analog power for MIPI DSI	1.7	1.9	V
DVDD18_MIPIRX	Analog power for MIPI CSI0	1.7	1.9	V
DVDD18_MIPIIO	Analog power for MIPI CSI1 & GPI	1.7	1.9	V
AVDD33_USB_P0	Analog power 3.3V for USB port 0	3.135	3.465	V
AVDD33_USB_P1	Analog power 3.3V for USB port 1	3.135	3.465	V
AVDD18_USB_P0	Analog power 1.8V for USB port 0	1.7	1.9	V
AVDD18_USB_P1	Analog power 1.8V for USB port 1	1.7	1.9	V
AVDD18_MEMPLL	Analog power for MEMPLL	1.7	1.9	V
DVDD18_NML1	Digital power input for NML1	1.62	1.98	V

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Symbol or pin name	Description	Min.	Max.	Unit
DVDD28_NML2	Digital power input for NML2	1.7	3.6	V
DVDD18_NML3	Digital power input for NML3	1.62	1.98	V
DVDD18_NML4	Digital power input for NML4	1.62	1.98	V
DVDD28_BPI	Digital power input for BPI	1.7	3.6	V
DVDD28_BSI	Digital power input for BSI	1.7	3.6	V
DVDD18_BSI	Digital power input for BSI	1.62	1.98	V
DVDD18_MC0	Digital power input for MSDC0	1.62	1.98	V
DVDD18_MC12	Digital power input for MSDC1/MSDC2	1.62	1.98	V
DVDD33_MC1	Digital power input for MSDC1	1.7	3.6	V
DVDD33_MC2	Digital power input for MSDC2	1.7	3.6	V
DVDD18_EMI	Digital power input for EMI	1.08	1.98	V
DVDD	Digital power input for core	0.95	1.15	V
DVDD_GPU	Digital power input for GPU	0.95	1.26	V
DVDD_DVFS	Digital power input for processor	0.77	1.26	V
DVDD_SRAM	Digital power input for processor memory	0.95	1.26	V

Warning: Stressing the device beyond the absolute maximum ratings may cause permanent damage. These are stress ratings only.

2.2.2 Recommended Operating Conditions

Table 2-5: Recommended operating conditions for power supply

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
DVDD18_PLLGP	Analog power input 1.8V for PLL	1.7	1.8	1.89	V
AVDD18_AP	Analog power input 1.8V for AuxADC, TSENSE	1.71	1.8	1.89	V
AVDD18_MD	Analog power input 1.8V for BBTX, BBRX, 2GBBTX	1.71	1.8	1.89	V
DVDD18_MD	Alternative analog power input 1.8V for BBTX, BBRX, 2GBBTX	1.71	1.8	1.89	V
AVDD28_DAC	Analog power input 2.8V for APC	2.66	2.8	2.94	V
DVDD18_MIPITX	Analog power for MIPI DSI	1.71	1.8	1.89	V
DVDD18_MIPIRX	Analog power for MIPI CSI0	1.71	1.8	1.89	V
DVDD18_MIPIIO	Analog power for MIPI CSI1 & GPI	1.71	1.8	1.89	V
AVDD33_USB_P0	Analog power 3.3V for USB port 0	3.135	3.3	3.465	V
AVDD33_USB_P1	Analog power 3.3V for USB port 1	3.135	3.3	3.465	V
AVDD18_USB_P0	Analog power 1.8V for USB port 0	1.71	1.8	1.89	V
AVDD18_USB_P1	Analog power 1.8V for USB port 1	1.71	1.8	1.89	V
AVDD18_MEMPLL	Analog power for MEMPLL	1.71	1.8	1.89	V
DVDD18_NML1	Digital power input for NML1	1.62	1.8	1.98	V
DVDD28_NML2	Digital power input for NML2	1.7	1.8	1.95	V
		2.7	3.3	3.6	
DVDD18_NML3	Digital power input for NML3	1.62	1.8	1.98	V

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Symbol or pin name	Description	Min.	Typ.	Max.	Unit
DVDD18_NML4	Digital power input for NML4	1.62	1.8	1.98	V
DVDD28_BPI	Digital power input for BPI	1.7	1.8	1.95	V
		2.7	3.3	3.6	
DVDD28_BSI	Digital power input for BSI	1.7	1.8	1.95	V
		2.7	3.3	3.6	
DVDD18_BSI	Digital power input for BSI	1.62	1.8	1.98	V
DVDD18_MC0	Digital power input for MSDC0	1.62	1.8	1.98	V
DVDD18_MC12	Digital power input for MSDC1/MSDC2	1.62	1.8	1.98	V
DVDD33_MC1	Digital power input for MSDC1	1.7	1.8	1.95	V
		2.7	3.3	3.6	
DVDD33_MC2	Digital power input for MSDC2	1.7	1.8	1.95	V
		2.7	3.3	3.6	
DVDD18_EMI	Digital power input for EMI (LPDDR2)	1.08	1.2	1.32	V
	Digital power input for EMI (UVDDR3)	1.125	1.25	1.375	
	Digital power input for EMI (LVDDR3)	1.215	1.35	1.485	
	Digital power input for EMI (DDR3)	1.35	1.5	1.65	
DVDD	Digital power input for core	1.00	1.05	1.10	V
DVDD_GPU	Digital power input for GPU	1.00	1.05	1.20	V
DVDD_DVFS	Digital power input for processor	0.81	1.15	1.20	V
DVDD_SRAM	Digital power input for processor memory	1.00	1.15	1.20	V

2.2.3 Storage Condition

1. Shelf life in sealed bag: 12 months at < 40°C and < 90% relative humidity (RH).
2. After bag opened, devices subjected to infrared reflow, vapor-phase reflow, or equivalent processing must be:
   - Mounted within 168 hours at factory conditions of 30°C/60% RH, or
   - Stored at 20% RH.
3. Devices require baking before mounting, if:
   - 192 hours at 40°C +5°C/-0°C and < 5% RH for low temperature device containers, or
   - 24 hours at 125°C +5°C/-0°C for high temperature device containers.

2.2.4 AC Electrical Characteristics and Timing Diagram

2.2.4.1 External Memory Interface for LPDDR2

The external memory interface, shown in Figure 2-4, Figure 2-5 and Figure 2-6, is used to connect LPDDR2 device for MT6589. It includes pins ED_CLK, ED_CLK_B, ECKE, ECS#, EBA[2:0], EDQS[3:0], EDQS#[3:0], EA[9:0] and ED[31:0]. Table 2-5 summarizes the symbol definition and the related timing specifications.

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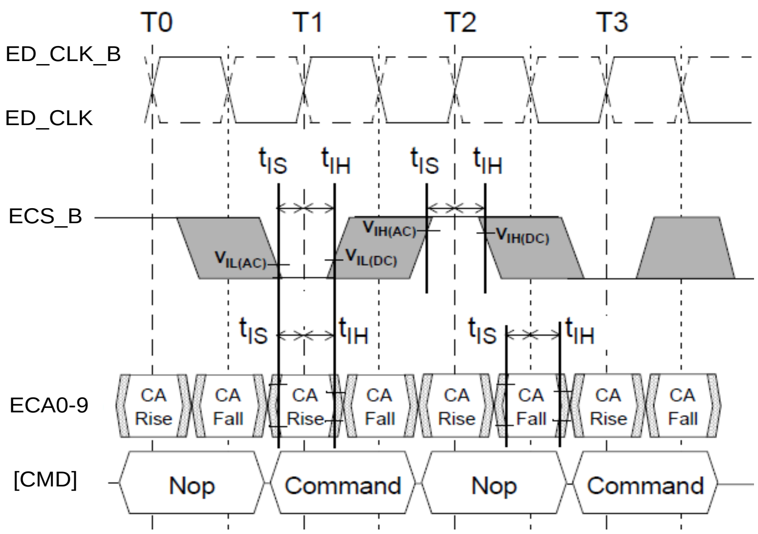

Figure 2-2: Basic timing parameter for LPDDR2 commands

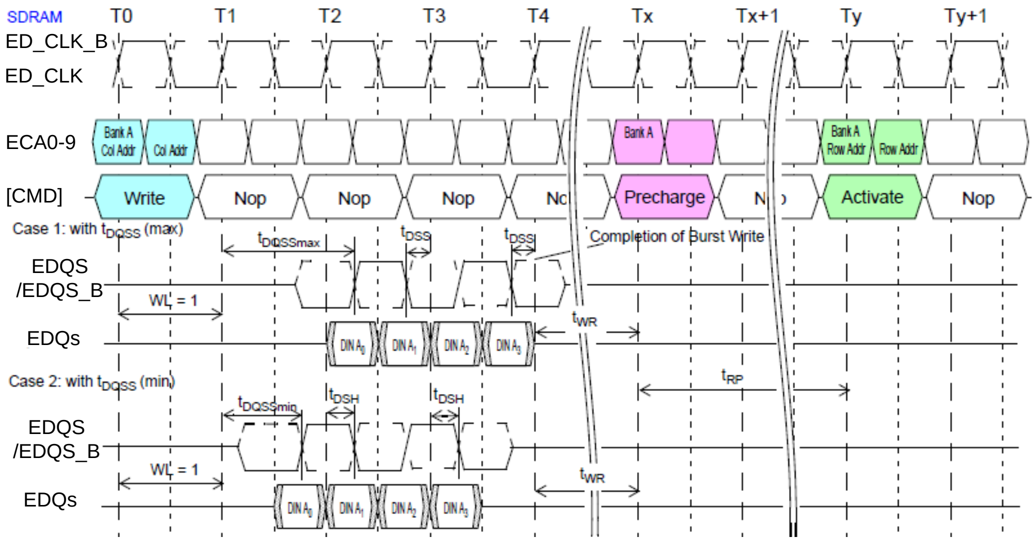

Figure 2-3: Basic timing parameter for LPDDR2 write

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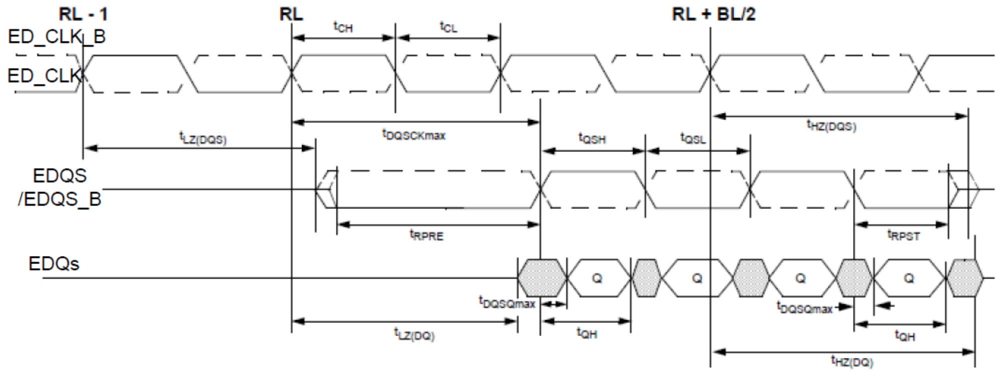
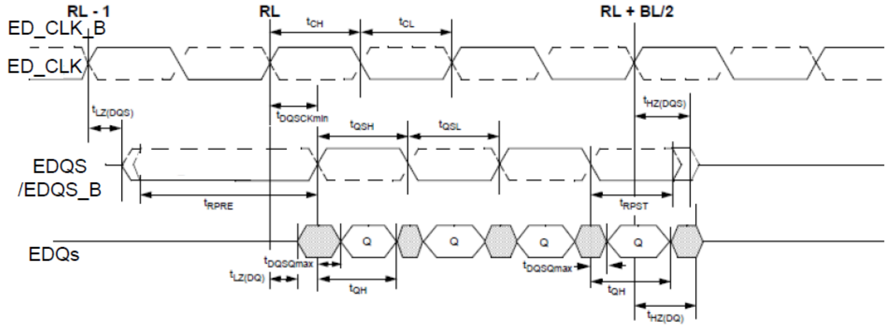


Data output (read) timing ($t_{DQSCKmax}$)



Data output (read) timing ($t_{DQSCKmin}$)

Figure 2-4: Basic timing parameter for LPDDR2 read

Table 2-6: LPDDR2 AC timing parameter table of external memory interfaces

Symbol	Description	Min.	Typ.	Max.	Unit
tCK	Clock cycle time	3.75		8	ns
tDQSCK	DQS output access time from CK/CK’	2.5		5.5	ns
tCH	Clock high level width	0.45		0.55	tCK
tCL	Clock low level width	0.45		0.55	tCK
tHP	Clock half period	0.45		0.55	tCK
tDS	DQ & DM input setup time	0.43			ns
tDH	DQ & DM input hold time	0.43			ns
tDQSS	Write command to 1^{st} DQS latching transition	0.75		1.25	tCK
tDSS	DQS falling edge to CK setup time	0.2			tCK
tDSH	DQS falling edge hold time from CK	0.2			tCK
tIS	Address & control input setup time	0.46			ns
tIH	Address & control input hold time	0.46			ns
tLZ(DQS)	DQS low-impedance time from CK/CK’	tDQSCK (Min.) – 300			ns
tHZ(DQS)	DQS high-impedance time from CK/CK’	tDQSCK (Max.) – 100			ns
tLZ(DQ)	DQ low-impedance time from CK/CK’	tDQSCK (Min.) – (1.4×tQHS (Max.))			ns
tHZ(DQ)	DQ high-impedance time from CK/CK’	tDQSCK (Max.) +			ns

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Symbol	Description	Min.	Typ.	Max.	Unit
		(1.4×tDQSQ (Max.))			
tDQSQ	DQS-DQ skew	0.34			ns
tQHP	Data half period	Min. (tQSH, tQSL)			tCK
tQHS	Data hold skew factor	0.4			ns
tQH	DQ/DQS output hold time from DQS	tQHP – tQHS			ns
tDQSH	DQS input high-level width	0.4			tCK
tDQSL	DQS input low-level width	0.4			tCK
tQSH	DQS output high pulse width	tCH – 0.05			tCK
tQSL	DQS output low pulse width	tCL – 0.05			tCK
tMRW	MODE register Write command period	5			tCK
tMRR	MODE register Read command period	2			tCK
tRPRE	Read preamble	0.9		1.1	tCK
tRPST	Read postamble	tCL – 0.05			tCK
tRAS	ACTIVE to PRECHARGE command period	3			tCK
tRC	ACTIVE to ACTIVE command period	6			tCK
tRFC	AUTO REFRESH to ACTIVE/AUTO REFRESH command period	56			tCK
tRCD	ACTIVE to READ or WRITE delay	3			tCK
tRP	PRECHARGE command period	3			tCK
tRRD	ACTIVE bank A to ACTIVE bank B delay	2			tCK
tWR	WRITE recovery time	3			tCK
tWTR	Internal write to READ command time	2			tCK
tXSR	SELF REFRESH exit to the next valid command	40			tCK
tXP	EXIT power-down to the next valid command delay	2			tCK
tCKE	CKE min. pulse width (high & low pulse width)	2			tCK

2.3 System Configuration

2.3.1 Mode Selection

Table 2-7: Mode selection of chip (PMU 6320 pin)

Pin name	Description
KP_COL0	0: Trigger USB download without battery 1: NA
KP_ROW0	0: Trigger USB download without battery 1: NA

2.3.1 Constant Tie Pins

Table 2-8: Constant tied pins of MT6589

Pin name	Description

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Pin name	Description
TESTMODE	Test mode (tie to GND)
FSOURCE_P	EFUSE burning (tie to GND)

2.4 Power-on Sequence

The power-on/off sequence with XTAL is shown in the following figure:

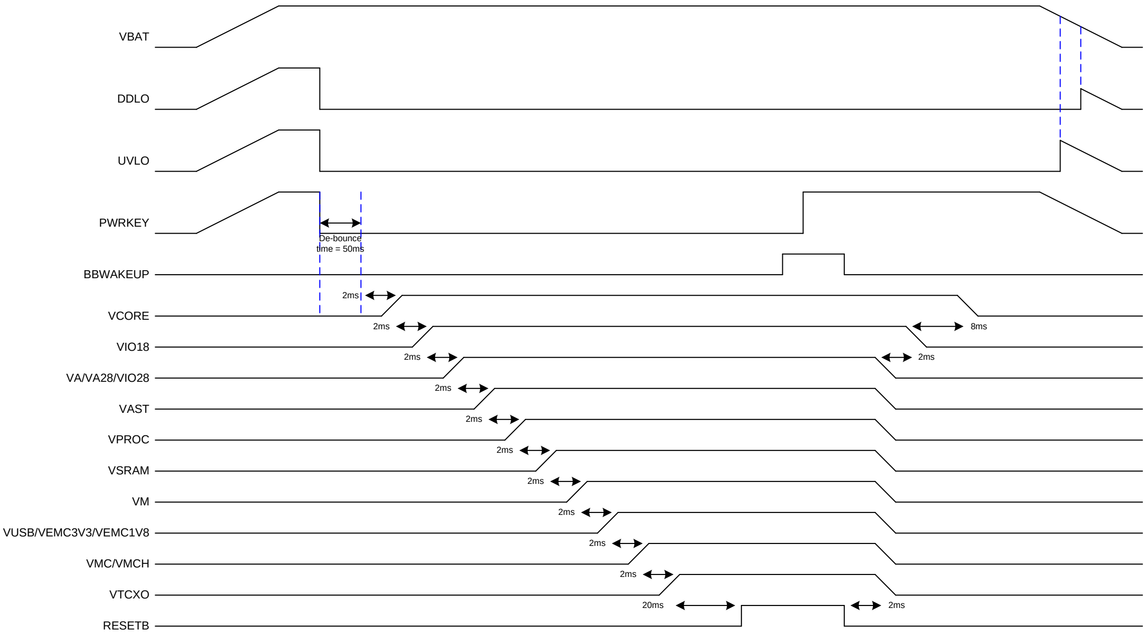

Figure 2-5: Power on/off sequence with XTAL

Note that the above figure only shows one power-on/off condition with XTAL. The external PMIC MT6320 for application processor MT6589 handles the power ON and OFF of the handset. The following three different methods switch on the handset (when VBAT ≥ 3.2V):

1. Pulling PWRKEY low (The user presses PWRKEY.)
2. Pulling BBWAKEUP high
3. Valid charger plug-in

Pulling PWRKEY low is a normal way to turn on the handset, which turns on regulators as long as the PWRKEY is kept low. MT6320 outputs reset signal RESETB to MT6589 SYSRSTB input. After SYSRSTB is de-asserted, the microprocessor starts and pulls BBWAKEUP high. After that PWRKEY can be released, pulling BBWAKEUP high will also turn on the handset. This is the case when the alarm in the RTC expires.

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Besides, applying a valid external supply on CHRIN will also turn on the handset. However, if the battery is in the UV state (VBAT < 3.2V), the handset cannot be turned on in any way.

The UVLO function in MT6320 prevents system startup when initial voltage of the main battery is below the 3.2V threshold. When the battery voltage is bigger than 3.2V, the UVLO comparator switches and threshold are reduced to 2.9V, which allows the handset to start smoothly unless the battery decays to 2.9V and below.

Once MT6320 enters the UVLO state, it draws very low quiescent current. The VRTC LDO will still be active until the DDLO disables it.

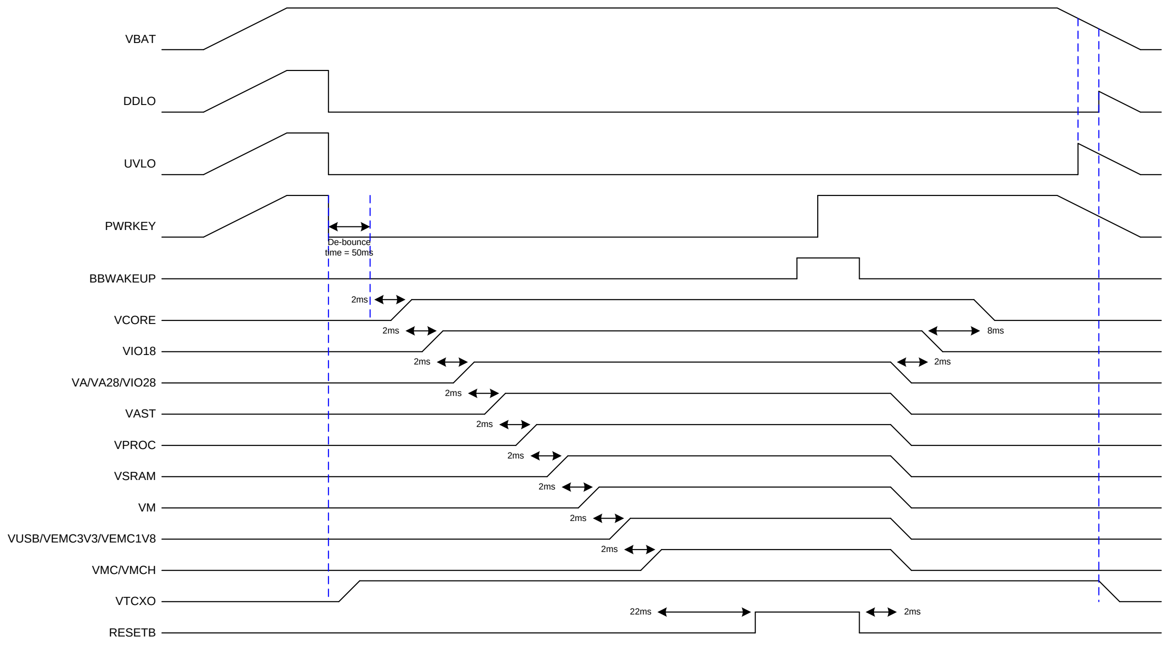

Figure 2-6: Power on/off sequence without XTAL

The figure above shows the power-on/off sequence without XTAL. VTCXO is always turned on when VBAT is above the DDLO threshold.

2.5 Analog Baseband

To communicate with analog blocks, a common control interface for all analog blocks is implemented. In addition, there are some dedicated interfaces for data transfer. The common control interface translates the APB bus write and read cycle for specific addresses related to analog front-end control. During the writing or reading of any of these control registers, there is a latency associated with the transfer of data to or from the analog front-end. Dedicated data interface of each analog block is implemented in the corresponding digital block. An analog block includes the following analog functions for the complete GSM/GPRS/WCDMA base-band signal processing:

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- Base-band Rx: For I/Q channels base-band A/D conversion
- Base-band Tx: For I/Q channels base-band D/A conversion and smoothing filtering.
- 2G base-band Tx: For the 2^{nd} I/Q channels base-band D/A conversion and smoothing filtering.
- RF control: Two DACs for automatic power control (APC) are included. Their outputs are provided to the external RF power amplifier respectively, according to the system dual-talk configuration. One more DAC for voltage bias control (VBIAS) is included for WCDMA system, and the output is provided to the external RF power amplifier.
- Auxiliary ADC: Provides an ADC for the battery and other auxiliary analog functions monitoring.
- Clock generation: Includes two clock-squarers for shaping the dual-talk system clock and 14 PLLs providing clock signals to base-band TRx, DSP, MCUUSB, MSDC, LVDS and HDMI units.

The analog blocks include the following analog functions for complete GSM/GPRS/WCDMA base-band signal processing:

- BBRX
- BBTX
- 2GBBTX
- APC-DAC
- VBIAS-DAC
- AUXADC
- Phase locked loop

2.5.1 BBRX

2.5.1.1 Block Descriptions

The receiver (Rx) performs baseband I/Q channels downlink analog-to-digital conversion:

1. Analog input multiplexer: For each channel, a 2-input multiplexer is included.
2. A/D converter: 4 high performance sigma-delta ADCs perform I/Q digitization for further digital signal processing.

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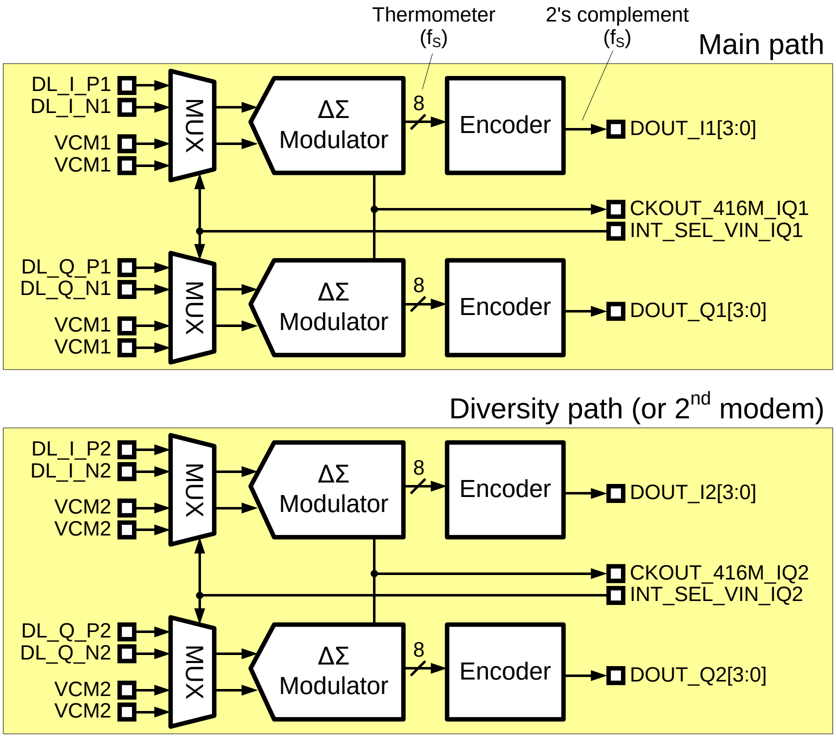

Figure 2-7: Block diagram of BBRX-ADC

2.5.1.2 Function Specifications

See the table below for the function specifications of the base-band downlink receiver.

Table 2-9: Baseband downlink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Differential analog input voltage (peak-to-peak)			2.4	V
ICM	Common mode input current magnitude			1	uA
VCM	Common mode input voltage	0.65	0.7	0.75	V
FC	Input clock frequency – Clock rate (DC mode) – Clock rate (SC mode & GSM mode)		 416 208		 MHz MHz
	Input clock duty cycle	49.5	50	50.5	%
	Input clock period jitter, DC mode			0.14	% (rms)
	Input clock period jitter, SC mode & GSM mode			0.61	% (rms)
RIN	Differential input resistance – DC mode – SC mode & GSM mode	 5.6 11.2	 8 16	 10.4 20.8	 kΩ kΩ
FS	Output sampling rate		416/208		MSPS
VOS	Differential input referred offset			10	mV
SIN	Signal to in-band noise – DC mode, 2.4Vpp (5.2MHz) sinewave, 400kHz ~ 4.6MHz band	72	75		dB

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	– SC mode, 2.4Vpp (2.7MHz) sinewave, 1kHz ~ 2.1MHz band – GSM mode: 2.4Vpp(570kHz) sinewave, 70kHz ~ 270kHz band	72 84	75 87		dB dB
DVDD18	Digital power supply	1.7	1.8	1.9	V
AVDD18	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	−20		80	°C
	Current consumption (per channel) – Power-up – Power-down			3 1	mA uA

2.5.2 BBTX

2.5.2.1 Block Descriptions

BBTX includes two channel DACs with the 1st order low pass filter. The DACs are PMOS current-steering topology with NMOS constant sinking current and the active RC filter performs current to voltage buffer.

The bitwidth of DACs is 10-bit which is encoded into 7 bits of thermometer code and 7 binary code by mixedsys hardware. The encoded bits are timing synchronized by D-type flip-flop which is toggled by the analog local clock. The MD-PLL delivers 832MHz differential clock to BBTX. A clock divider translates the 832MHz to 416MHz for DACs and AFIFO inside mixedsys.

The IO power, DVDD18_MD is regulated to a voltage around 1.55V to supply analog component. The required bias currents are generated by BBRX.

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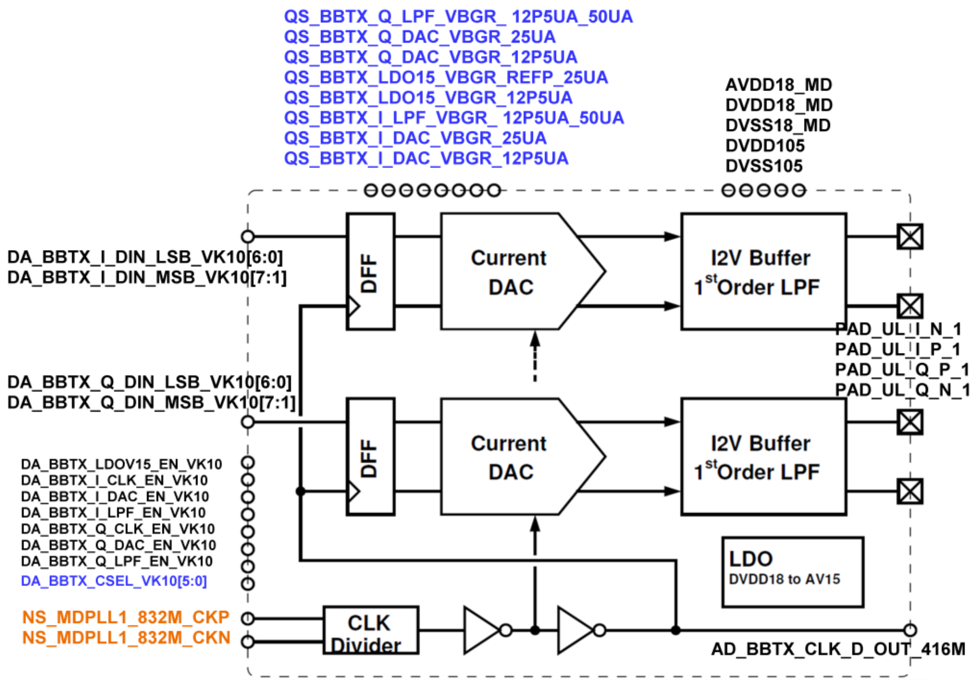

2.5.2.2 Function Specifications

Table 2-10: Baseband uplink transmitter specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{ocm}	DC output common mode voltage	0.615	0.65	0.685	V
I_K	HF leakage current @ supply, Irms @416*2 = 832MHz			3.5	uA
V_{fs}	DAC output swing		2100		mV
N	DAC resolution		10.0		bit
F_s	Sampling clock		416		MHz
I_{mis}	1-sgma DAC unit cell mismatch			1	%
G_{mis}	3-sigma I/Q gain mismatch	-0.2		0.2	dB
V_{os_T}	3-sigma output differential DC offset over temp.			4	mV
V_{os}	3-sigma output differential DC offset			10	mV
F_{3dB}	3dB corner freq.	20	25	30	MHz
S_{LPF}	LPF selectivity @832MHz	28			dB
N_{OOB}	Output noise level @45MHz		15.1	30.1.	nVrms/sqrt(Hz)
CN	Signal to noise ratio@45MHz		-146	-140	dBc/Hz
IM3	In-band two-tone test swing V1=V2=290/sqrt(2) mV		-60	-56	dBc
T	Operating temperature	-20		80	°C
	Current consumption – Power-up – Power-down		 4.1 10		 mA uA

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2.5.3 2GBBTX

2.5.3.1 Block Descriptions

The 2G transmitter (2GTx) performs 2G baseband I/Q channels up-link digital-to-analog conversion for dual-talk application. Each channel includes:

1. 11-bit D/A converter: Converts digital modulated signals to analog domain. The input to the DAC is sampled at 26 MHz rate with the 11-bit resolution.
2. Smoothing filter: The low-pass filter performs smoothing function for DAC output signals with a 1.8MHz 2nd-order Butterworth frequency response.

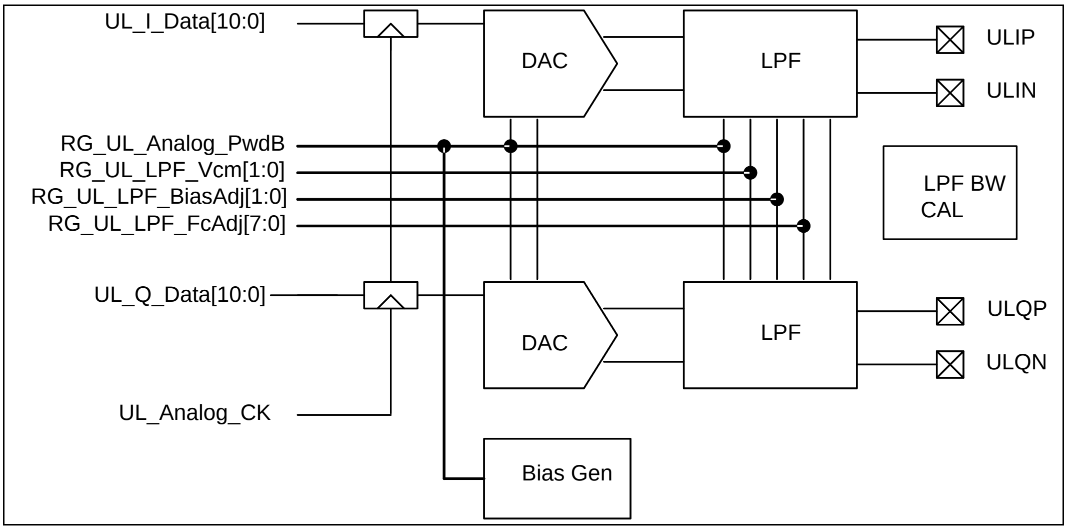

Figure 2-8: Block diagram of 2GBBTX

2.5.3.2 Function Specifications

See the table below for the function specifications of the 2G base-band uplink transmitter.

Table 2-11: Baseband uplink transmitter specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		11		Bit
FS	Sampling rate		26		MSPS
SINAD	Signal to noise and distortion ratio (in-band)		80		dB
THD	Total harmonic distortion		-60		dB
	Output swing (full Swing)	0.9	1.0	1.1	Vppd
VOCM	Output CM voltage	1.05	1.1	1.15	V
	Output capacitance (single-ended)			20	PF
	Output resistance (differential)		1.5		KΩ
DNL	Differential nonlinearity	-0.5		+0.5	LSB
INL	Integral nonlinearity	-1.0		+1.0	LSB

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Symbol	Parameter	Min.	Typ.	Max.	Unit
OE	Offset error (after calibration)		+/- 1		LSB
FCUT	Filter -3dB cutoff frequency (calibrated)		1.8		MHz
	I/Q gain mismatch		+/- 0.2		dB
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption – Power-up – Power-down		 3.6 10		 mA uA

2.5.4 APC-DAC

2.5.4.1 Block Descriptions

See the figure below. APC-DAC is designed to produce a single-ended output signal at APC pin.

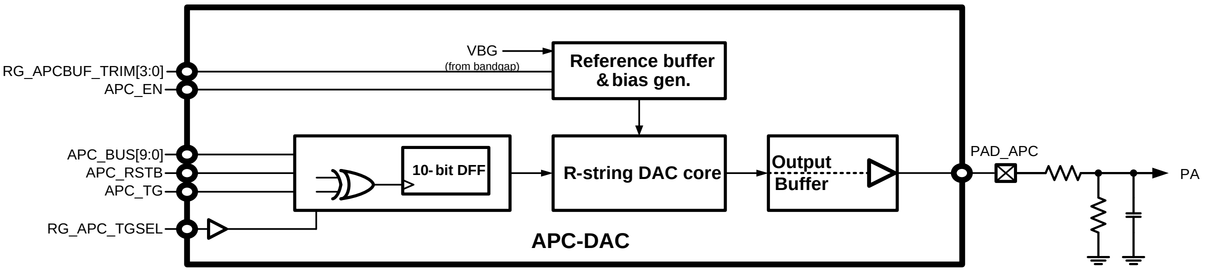

Figure 2-9: Block diagram of APC-DAC

2.5.4.2 Function Specifications

See the table below for the function specifications of the APC-DAC.

Table 2-12: APC-DAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
F_S	Clock rate	1.0833		2.1666	MS/s
SNDR	Signal-to-noise-and-distortion ratio (10kHz sine wave with 1.0V swing)		50		dB
T_S	Settling time (99% full-swing settling)			5	us
$V_{O,max}$	Maximum output			AVDD – 0.2	V
C_L	Output loading capacitance		1,000	2,200	pF
DNL	Differential nonlinearity (code 30 ~ 970)		±1.0		LSB
INL	Integral nonlinearity (code 30 ~ 970)		±2.0		LSB
DVDD	Digital power supply	0.9	1.0	1.1	V
AVDD	Analog power supply	2.6	2.8	3.0	V

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Symbol	Parameter	Min.	Typ.	Max.	Unit
T	Operating temperature	–20		85	°C
I_{ON}	Current consumption (power-on state)		300		uA
I_{OFF}	Current consumption (power-down state)			1	uA

2.5.5 VBIAS-DAC

2.5.5.1 Block Descriptions

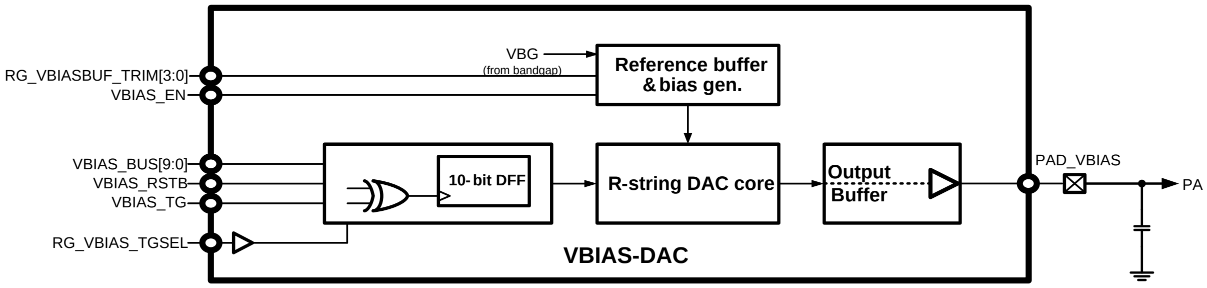

Figure 2-10: Block diagram of VBIAS-DAC

2.5.5.2 Function Specifications

The functional specifications of the VBIAS-DAC are listed in the following table.

Table 2-13: VBIAS-DAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
F_S	Clock rate	1.0833		2.1666	MS/s
SNDR	Signal-to-noise-and-distortion ratio (10KHz sine wave with 1.0V swing)		50		dB
T_S	Settling time (99% full-swing settling)			5	us
$V_{O,max}$	Maximum output			AVDD – 0.2	V
C_L	Output loading capacitance		1000		pF
DNL	Differential nonlinearity (code 20 ~ 970)		±1.0		LSB
INL	Integral nonlinearity (code 20 ~ 970)		±2.0		LSB
DVDD	Digital power supply	0.9	1.0	1.1	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	–20		85	°C
I_{ON}	Current consumption (power-on state)		300		uA
I_{OFF}	Current consumption (power-down state)			1	uA

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2.5.6 AUXADC

2.5.6.1 Block Descriptions

Auxiliary ADC measures ADC and is the resistive touch panel controller. The auxiliary ADC includes the following functional blocks:

1. Analog multiplexer: Selects signal from one of the auxiliary input channels. There are 16 input channels of AUXADC. Some are for internal voltage measuring and some for external voltage measuring. Environmental messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
2. 12-bit A/D converter: Converts the multiplexed input signal to 12-bit digital data.

The touch screen controller drives the external touch panel via Pads XP, XM, YP and YM, and AUXADC as a voltage meter, obtains the X/Y-position of the touched point on the external touch screen. The touch screen interface contains 3 main blocks, which are touch screen pads control logic, ADC interface logic and interrupt generation logic. The touch screen interface supports 2 conversion modes, separate X/Y position conversion mode and auto (sequential) X/Y position conversion mode. See

Table ***2-14: Definitions of AUXADC channels*** for brief descriptions of AUXADC input channels.

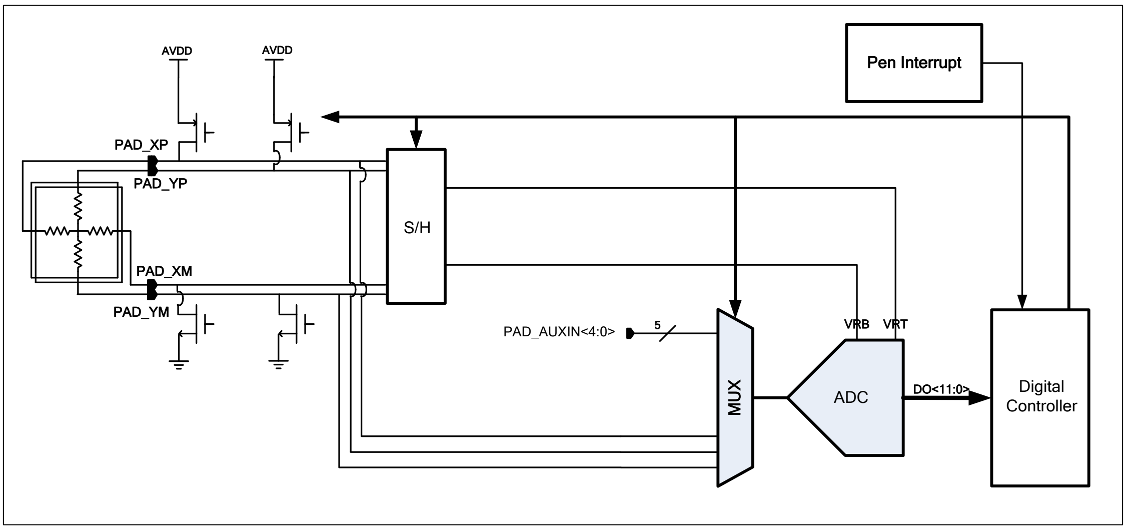

Figure 2-11: Block diagram of AUXADC

Table 2-14: Definitions of AUXADC channels

AUXADC channel ID	Description
Channel 0	External use (AUX_IN0)
Channel 1	External use (AUX_IN1)
Channel 2	Optional external use (AUX_IN2)

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AUXADC channel ID	Description
Channel 3	Optional external use (AUX_IN3)
Channel 4	Optional external use (AUX_IN4)
Channel 5	NA
Channel 6	NA
Channel 7	NA
Channel 8	NA
Channel 9	NA
Channel 10	NA
Channel 11	NA
Channel 12	XM (touch panel)
Channel 13	XP (touch panel)
Channel 14	YP (touch panel)
Channel 15	YM (touch panel)

2.5.6.2 Function Specifications

See the table below for the function specifications of auxiliary ADC.

Table 2-15: AUXADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		12		Bit
FC	Clock rate		4		MHz
FS	Sampling rate @ N-Bit		4/(N+4)		MSPS
	Input swing	0		AVDD	V
CIN	Input capacitance Unselected channel Selected channel		 50 4		 fF pF
RIN	Input resistance Unselected channel	 400			 MΩ
	Clock latency		N+4		1/FC
DNL	Differential nonlinearity		+1.0/-1.0		LSB
INL	Integral nonlinearity		+1.0/-1.0		LSB
OE	Offset error		+/- 5		mV
FSE	Full swing error		+/- 5		mV
SINAD	Signal to noise and distortion ratio (10kHz full swing input & 1.0833MHz clock rate)	62	68		dB
DVDD	Digital power supply	1.0	1.1	1.2	V
AVDD	Analog power supply	1.75	1.8	1.85	V
T	Operating temperature	-20		80	°C
	Current consumption – Power-up – Power-down		 250 1		 uA uA
Ztp	Supports touch panel impedance	200		2K	Ω

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2.5.7 Clock Squarer

2.5.7.1 Block Descriptions

For most VCXO, the output clock waveform is sinusoidal with too small amplitude (about several hundred mV) to make MT6589 digital circuits function well. Clock squarer is designed to convert such a small signal to a rail-to-rail clock signal with excellent duty-cycle.

2.5.7.2 Function Specifications

See the table below for the function specifications of clock squarer.

Table 2-16: Clock squarer 1 & 2 specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency	13	26		MHz
Fout	Output clock frequency	13	26		MHz
Vin	Input signal amplitude	350	500	1,000	mVpp
DcycIN	Input signal duty cycle		50		%
DcycOUT	Output signal duty cycle	DcycIN-5		DcycIN+5	%
TR	Rise time on pin CLKSQOUT			5	ns/pF
TF	Fall time on pin CLKSQOUT			5	ns/pF
DVDD	Digital power supply	1.0	1.1	1.2	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	℃
	Current consumption		500		uA

2.5.8 Phase Locked Loop

2.5.8.1 Block Descriptions

There are total 14 PLLs in PLL macro, providing several clocks for CPU, BUS, modem, analog modem, MSDC, LVDS, HDMI and image-sensor. ARMPLL provides around 1.2GHz clock for ARM Cortex-A15. MAINPLL provides around 806MHz clock for bus and most of the function modules. MMPLL provides around 286MHz clock for VENC and MFG. ISPPLL is the clock source of image sense processing, which ranges from 104 to 208MHz for supporting various image sensors. UNIVPLL provides 48MHz for USBPHY. MSDCPLL provides around 208MHz as the clock source of MSDC module. TVDPLL provides 27/54/148.5MHz clock for the TV encoder and HDMI bridge. LVDSPLL provides 20 ~ 75MHz clock for LVDS bridge and DPI interface. MDPLL1 and MDPLL2 are the main clock source of dual-talk modem, providing a fixed 416MHz from different clock squarers for further clock division. WPLL is a fractional PLL which multiplies clock 26MHz to 245.76MHz for HSPA. WHPLL provides a fixed 250.25MHz for 3G HSPA. MCUPLL1 and MCUPLL2 provide around 481MHz for ARM Cortex-R4, FD216 and bus.

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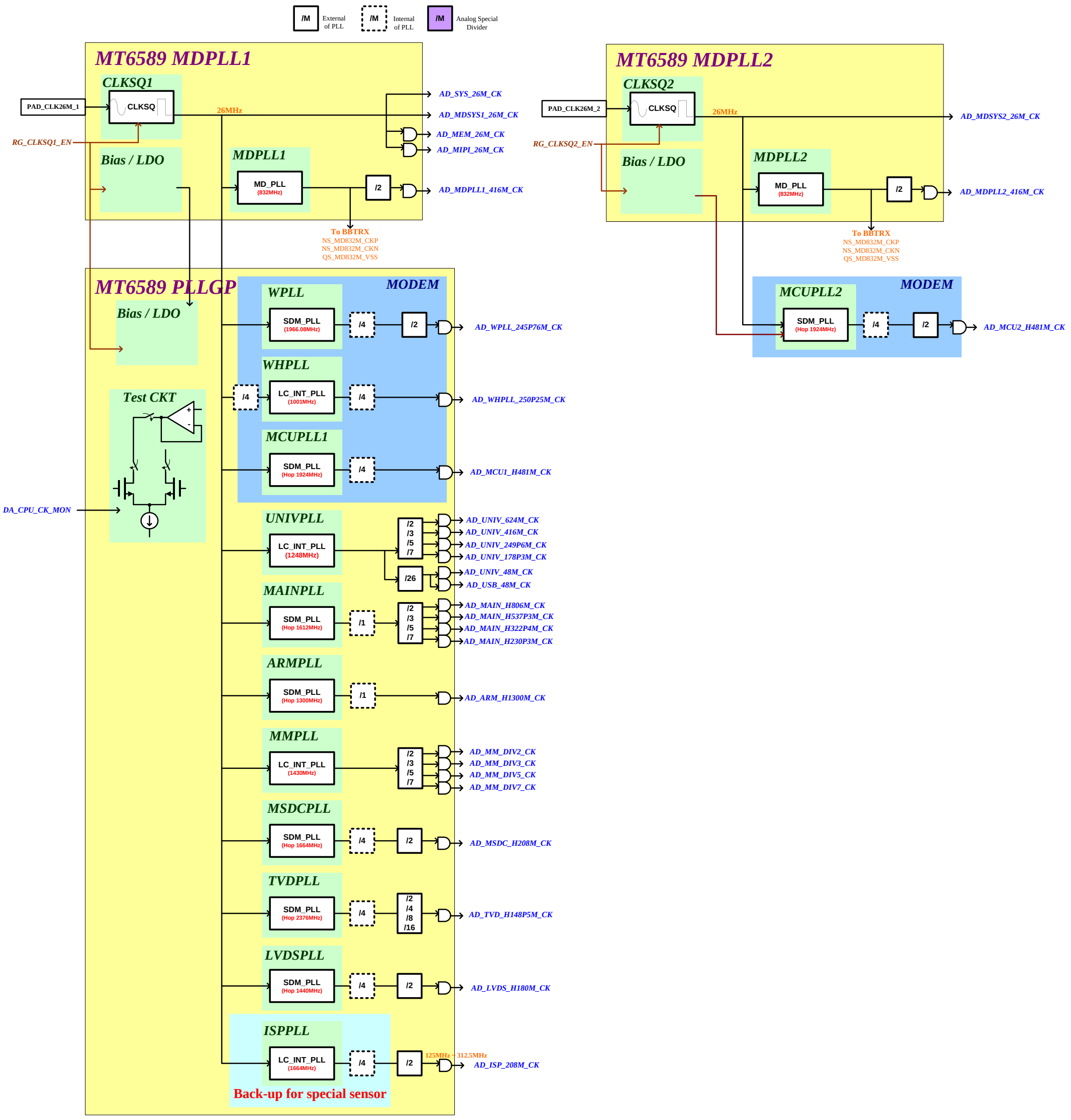

Figure 2-12: Block diagram of PLL

2.5.8.2 Function Specifications

See the table below for the function specifications of PLL.

Table 2-17: ARMPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	754		1,508	MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		30		ps
DVDD	Digital power supply	0.95	1.05	1.15	V

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Symbol	Parameter	Min.	Typ.	Max.	Unit
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1.2		mA
	Power-down current consumption			1	uA

Table 2-18: MAINPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	500	806	884	MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-19: MMPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		286	338	MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-20: ISPPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	104		208	MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-21: UNIVPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	624	N/A	MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-22: MSDCPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		208		MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-23: TVDPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		148.5		MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

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Table 2-24: LVDSPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		75		MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-25: MDPLL1 & MDPLL2 specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	416	N/A	MHz
	Settling time		100		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		30		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		2.5		mA
	Power-down current consumption			1	uA

Table 2-26: WPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	245.76	N/A	MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-27: WHPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz

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Symbol	Parameter	Min.	Typ.	Max.	Unit
Fout	Output clock frequency	N/A	250.25	N/A	MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-28: MCUPLL1 & MCUPLL2 specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		481		MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		2		mA
	Power-down current consumption			1	uA

2.5.9 Temperature Sensor

2.5.9.1 Block Descriptions

In order to monitor the temperature of CPUs, several temperature sensors are provided. The temperature sensor is made of substrate BJT in the CMOS process. The voltage output of temperature sensor is measured by AUXADC.

2.5.9.2 Function Specifications

See the table below for the function specifications of temperature sensor.

Table 2-29: Temperature sensor specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Resolution		0.15		°C
	Temperature range	0		85	°C
	Accuracy	-5		5	°C
	Active current		300		uA
	Quiescent current		3		uA

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2.6 Package Information

2.6.1 Package Outlines

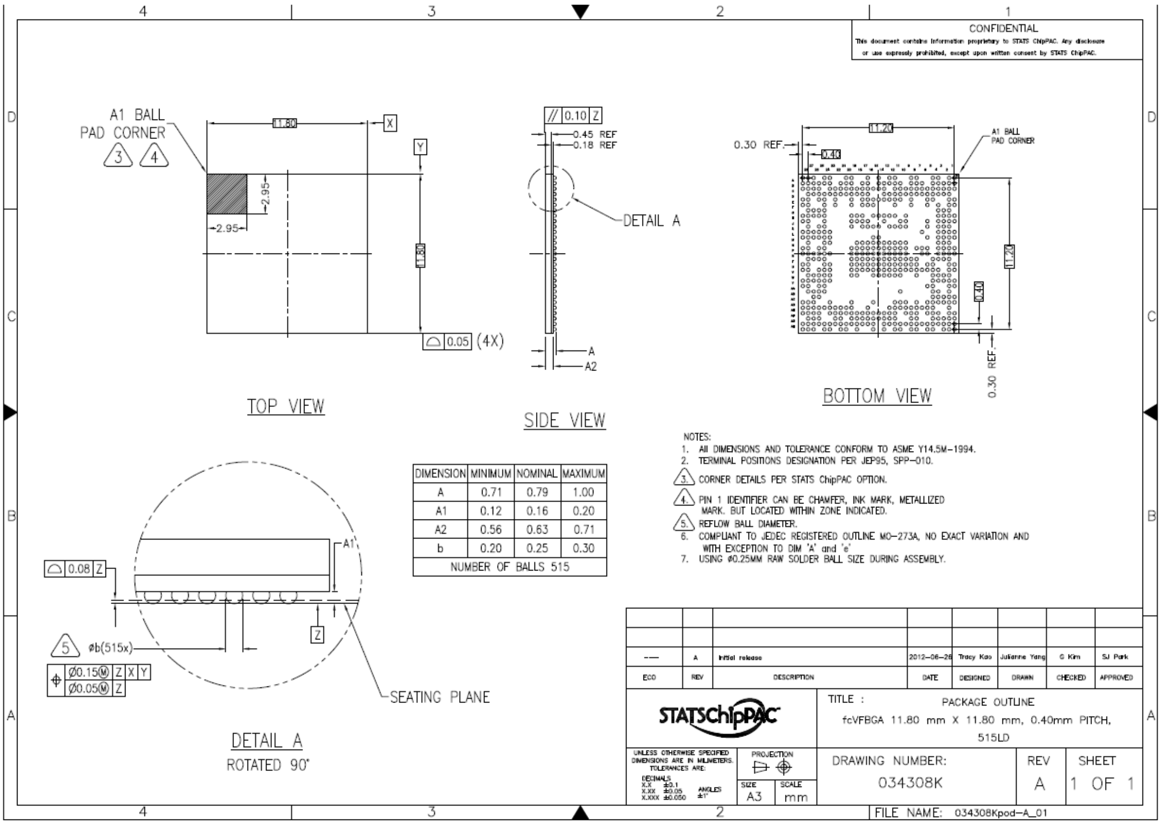

*Figure 2-13: Outlines and dimensions of FCCSP 11.8mm*11.8mm, 515-ball, 0.4mm pitch package*

2.6.2 Thermal Operating Specifications

Table 2-30: Thermal operating specifications

Symbol	Description	Value	Unit	Notes
	Maximum operating junction temperature	125	°C	
	Package thermal resistances in nature convection	29.55	°C/Watt	

2.6.3 Lead-free Packaging

MT6589 is provided in a lead-free package and meets RoHS requirements.

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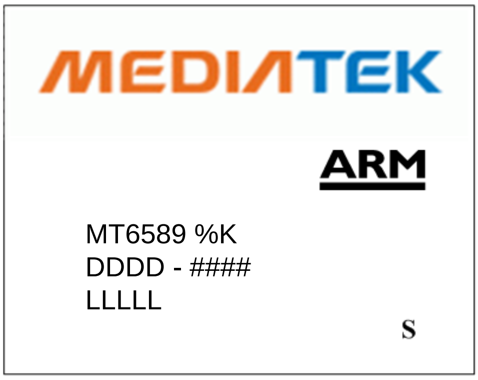
2.7 Ordering Information

2.7.1 Top Marking Definition



MTXXXXXX	Part No.
%:	W : WCDMA T : TD-SCDMA E : Edge
DDDD:	Date Code
####:	Subcontractor Code
LLLLL:	Die Lot No.
S:	Special Code

Figure 2-14: Top mark of MT6589

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